IS29GL064
IS29GL032
IS29GL016

64Mb/32Mb/16Mb
3.0V PAGE MODE PARALLEL FLASH MEMORY

ADVANCED DATA SHEET

IS29GL064/032/016
64/32/16 Megabit Flash Memory
Page mode Flash Memory, CMOS 3.0 Volt-only

ADVANCED INFORMATION

FEATURES

- Supply operation
- V_{CC} = 2.7~3.6V
- V_{CCQ} = 1.65~3.6V (I/O buffers)
- V_{PPH} = 9.5~10.5V (Vpp/WP#))

- Asynchronous random or page read
- Page size: 8 words or 16 bytes
- Page access: 25ns
- Random access (V_{CCQ} = 2.7~3.6V):60ns (BGA); 70ns (TSOP)

- Buffer program: 256-word MAX program buffer

- Program time
  - 0.56us per byte (1.8MB/s TYP when using 256-word buffer size in buffer program without V_{PPH})
- 0.31us per byte (3.2MB/s TYP when using 256-word buffer size in buffer program with V_{PPH})

- Memory Organization
  - 16Mb: 32x 64KB (Uniform), or 8x 8KB (Top or Bottom Boot)+31x64KB
  - 32Mb: 64x 64KB (Uniform), or 8x 8KB (Top or Bottom Boot)+63x64KB
  - 64Mb: 128x 64KB (Uniform), or 8x 8KB (Top or Bottom Boot)+127x64KB

- Program/erase suspend and resume capability
  - Program suspend: Read from another block
  - Erase suspend: Read or Program from another block

- BLANK CHECK operation to verify an erased block

- Unlock bypass, block erase, chip erase, and write to buffer capability
- Fast buffered/batch programming
- Fast block and chip erase

- VPP/WP# pin protection
  - V_{PPH} voltage on VPP to accelerate programming performance
  - Protects highest/lowest block (H/L uniform) or top/bottom two blocks (T/B boot)

- Software Protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
  - Password access

- Support CFI (Common Flash Interface)

- Extended Memory block
  - 128-word (256-byte) block for permanent secure identification
  - Program or lock implemented at the factory or by customer

- Low Power consumption: Standby mode

- Data retention: 20 years (TYP)

- 100K minimum ERASE cycles per block

- Package Options
- 48-pin TSOP
- 56-pin TSOP
- 64-ball 11mm x 13mm BGA
- 48-ball 6mm x 8mm BGA

- Temperature Range
- Extended Grade: -40°C to +105°C
- Automotive A3 Grade: -40°C to +125°C

GENERAL DESCRIPTION

The IS29GL064/032/016 offer fast page access time of 25ns with a corresponding random access time as fast as 60ns. It features a Write Buffer that allows a maximum of 256 words/512 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes the device ideal for today's embedded applications that require higher density, better performance and lower power consumption.

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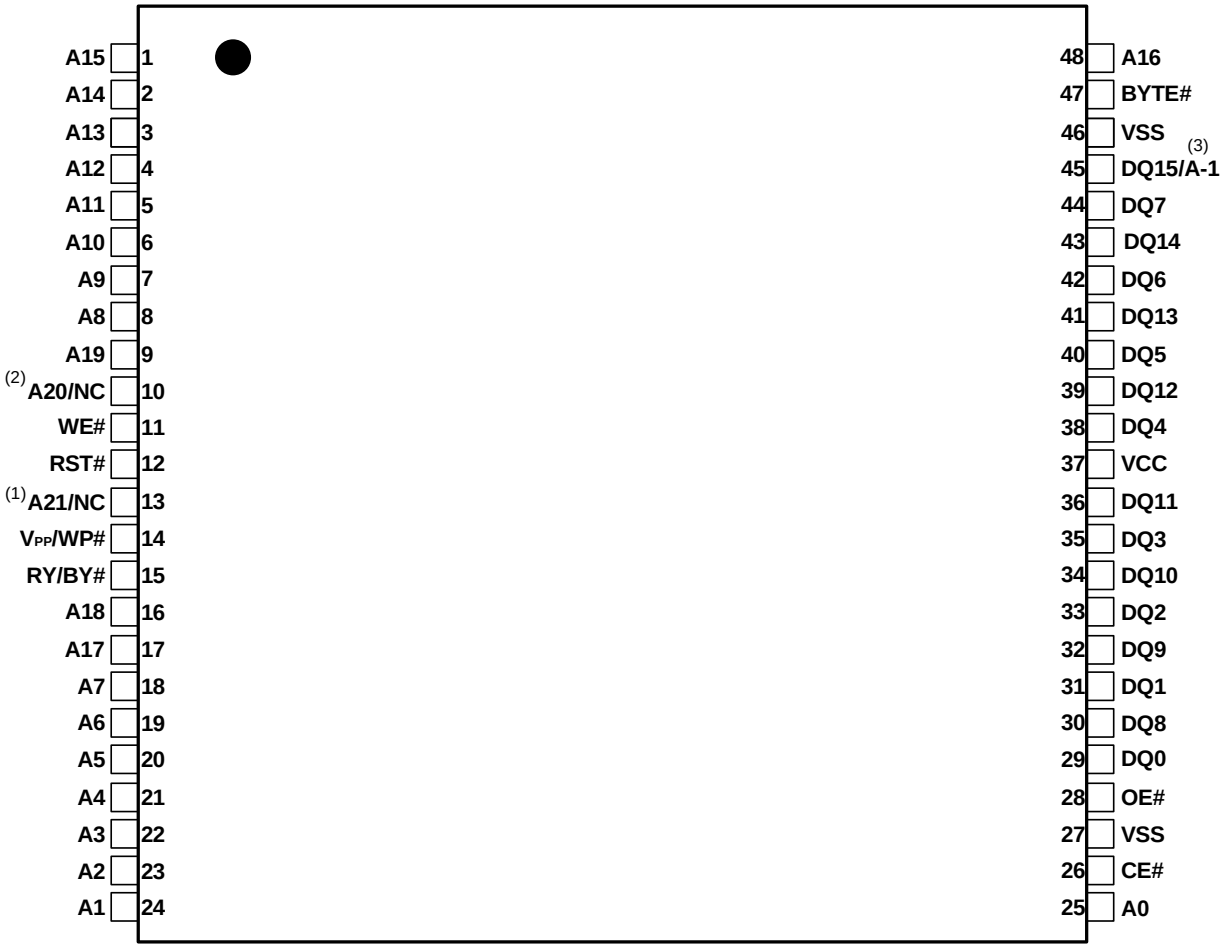
PIN CONFIGURATION

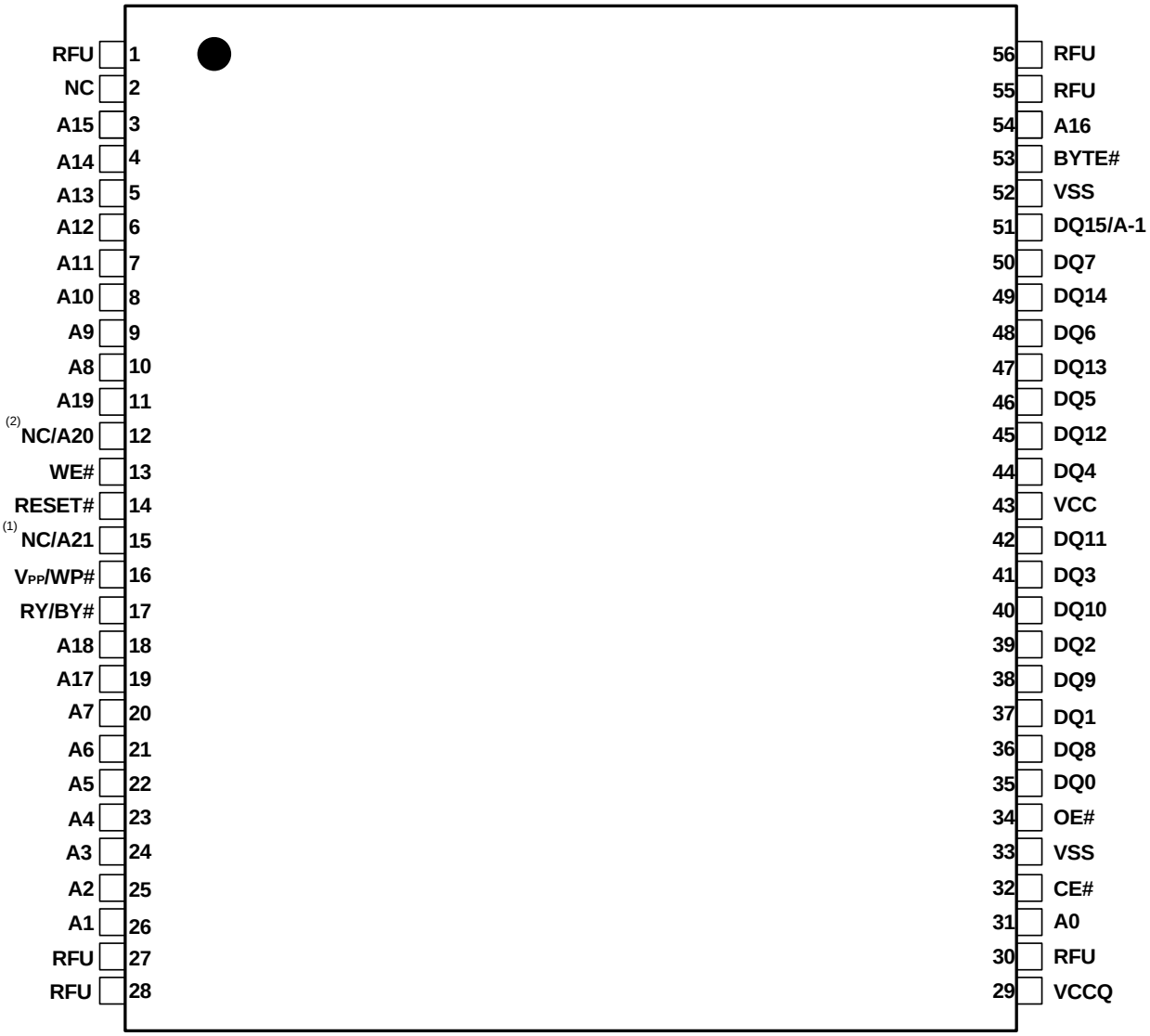
Figure 1. 48-pin TSOP (Top View), (PKG Code: T)



Notes:

1. A21 is valid for 64Mb, and it is NC in 32Mb/16Mb
2. A20 is valid for 64/32Mb, and it is NC in 16Mb
3. A-1 is the least significant address in x8 mode
4. For 48-pin, there is no V_{CCQ} pin. Vcc also supply IO, it can only be 2.7~3.6V

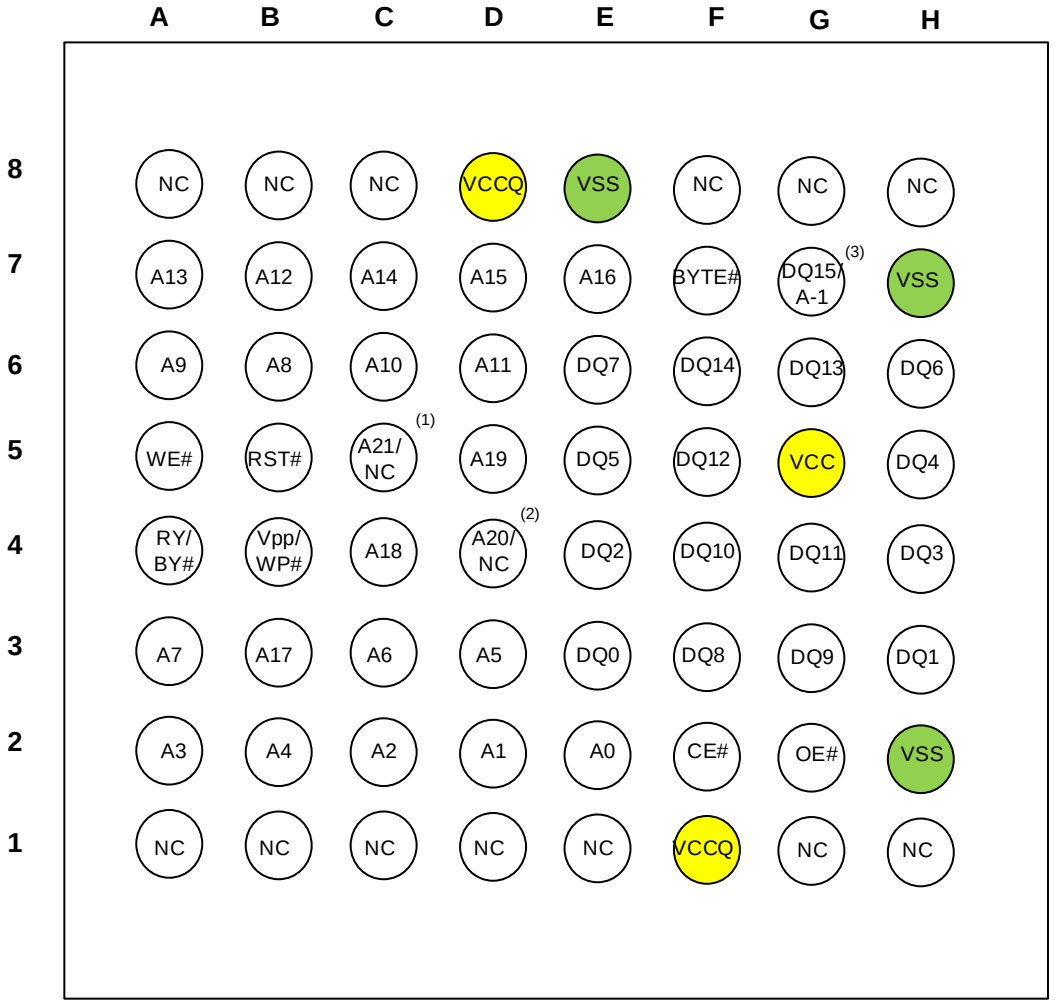
Figure 2. 56-pin TSOP (Top View), (PKG Code: S)



Notes:

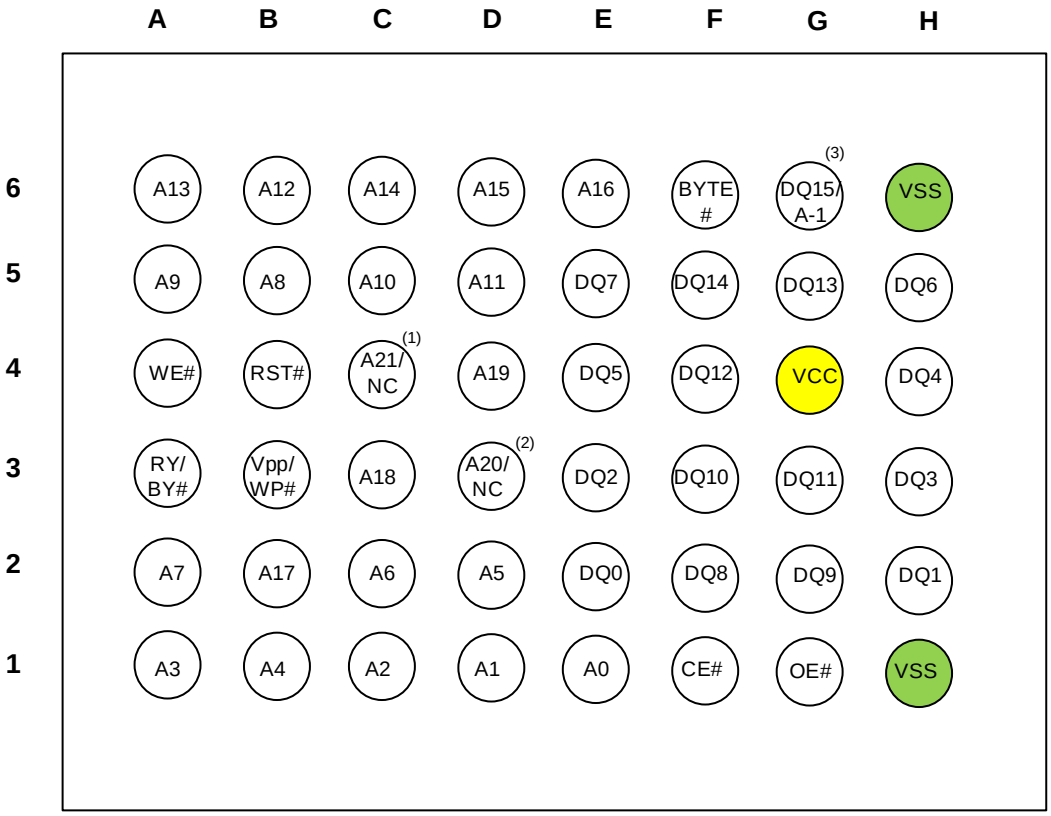
1. A21 is valid for 64Mb, and it is NC in 32Mb/16Mb
2. A20 is valid for 64/32Mb, and it is NC in 16Mb
3. A-1 is the least significant address in x8 mode

Figure 3. 64-ball Ball Grid Array (Top View, Balls Facing Down), (PKG Code: F)



Notes:
1. A21 is valid for 64Mb, and it is NC in 32Mb/16Mb
2. A20 is valid for 64/32Mb, and it is NC in 16Mb
3. A-1 is the least significant address in x8 mode

Figure 4. 48-ball Ball Grid Array (Top View, Balls Facing Down)



Notes:

1. A21 is valid for 64Mb, and it is NC in 32Mb/16Mb
2. NA20 is valid for 64/32Mb, and it is NC in 16Mb
3. A-1 is the least significant address in x8 mode
4. For 48-ball, there is no V_{CCQ} pin. Vcc also supply IO, it can only be 2.7~3.6V

TABLE 1. PIN DESCRIPTION

Pin Name	Function
A21–A0	22 Address Inputs for 64Mb
A20–A0	21 Address Inputs for 32Mb
A19–A0	20 Address Inputs for 16Mb
DQ7-DQ0	Data inputs/outputs.
DQ14-DQ8	Outputs data during a read operation when BYTE# is HIGH. High-Z when BYTE# is LOW. During write operations, these bits are not used.
DQ15 / A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
CE#	Chip Enable
OE#	Output Enable
RST#	Hardware Reset Pin
RY/BY#	Ready/Busy Output
WE#	Write Enable
Vcc	Supply Voltage
Vss	Ground
V_{CCQ}	Supply Voltage for Input/Output.
BYTE#	Byte/Word mode selection
Vpp/WP#/	Write Protect and V_{PPH} function. These functions protect the lowest or highest block or top two blocks or bottom two blocks, enable the device to enter unlock bypass mode and accelerated program speed, respectively. A 0.1uF capacitor should be connected between Vpp/WP# and VSS to decouple the current surges from the power supply when VPPH is applied. (WP# has an internal pull-up; when unconnected, WP# is at V_{IH}.)
NC	No Connect

FIGURE 5. LOGIC DIAGRAM

64Mb/32/16Mb Logic Symbol

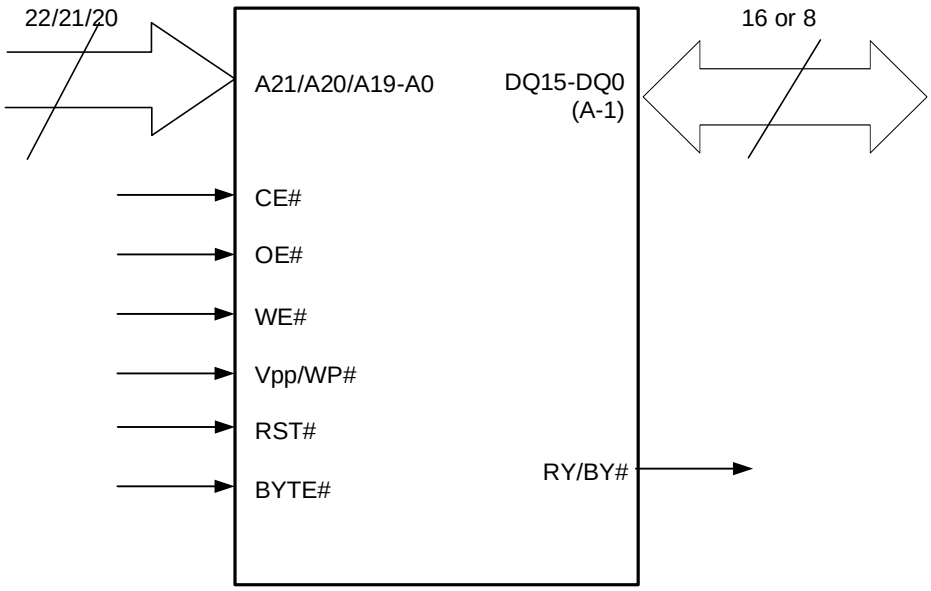


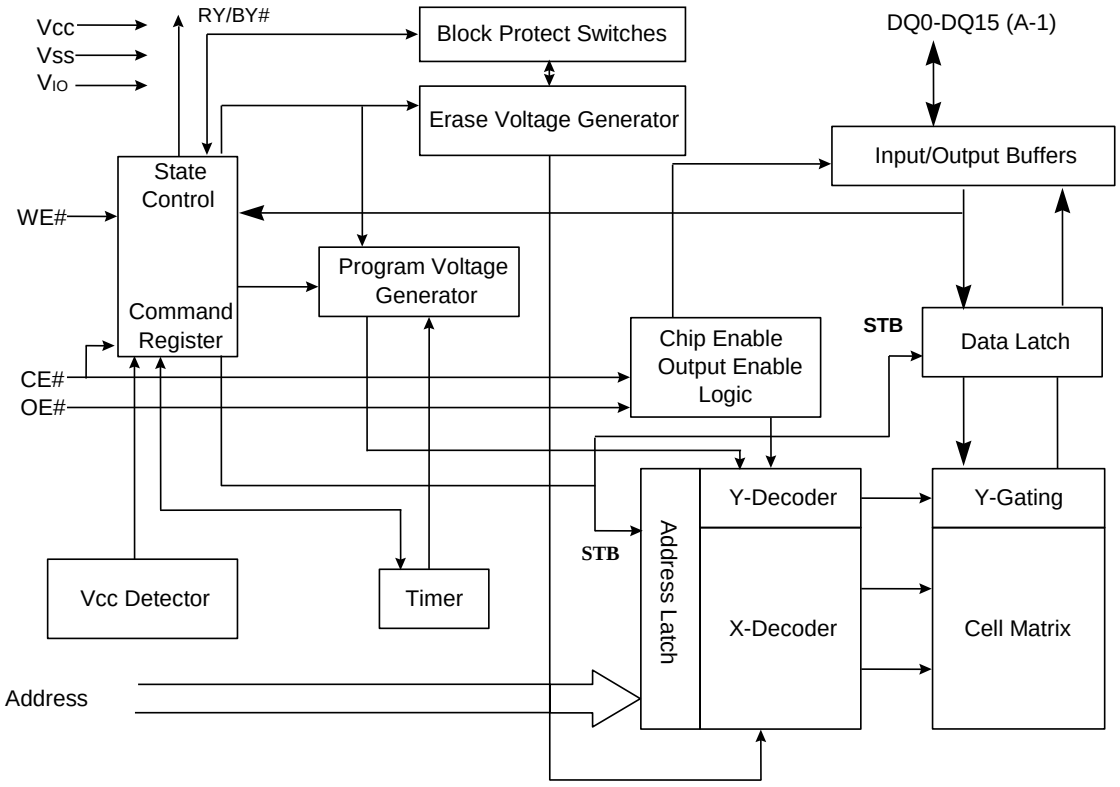
Table 2. PRODUCT SELECTOR GUIDE

- Speed bin depends on package type.

Supply Voltage for Input/Output & Package		IS29GL064/032/016	
		Temperature	
		-40°C to +105°C	-40°C to +125°C
V_{CCQ} = 2.7 – 3.6 V (1)	BGA	**60ns**	**60ns**
	TSOP	**70ns**	**70ns**

Note:
1. Speed will be slower by 5ns when V_{CCQ} < 2.7V: 60ns→65ns, 70ns→75ns
2. No V_{CCQ} pin for 48-pin TSOP and 48-ball BGA.

FIGURE 6. BLOCK DIAGRAM



Memory Configuration

- The 64Mb device (x8/x16) can be divided into 127 main blocks (64KB each) and 8 top or bottom boot blocks (8KB each).
  It is also divided into 128 main uniform blocks (64KB each)

- The 32Mb device (x8/x16) can be divided into 63 main blocks (64KB each) and 8 top or bottom boot blocks (8KB each).
  It is also divided into 64 main uniform blocks (64KB each)

- The 16Mb device (x8/x16) can be divided into 31 main blocks (64KB each) and 8 top or bottom boot blocks (8KB each).
  It is also divided into 32 main uniform blocks (64KB each)

Table 3. 64Mb Memory Map – x8 Top and Bottom Boot [134:0]

Block	Block Size	Address Range (x8 Top Boot)		Block	Block Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
134	8KB	007F E000	007F FFFF	134	64KB	007F 0000	007F FFFF
133		007F C000	007F DFFF	133		007E 0000	007E FFFF
132		007F A000	007F BFFF	132		007D 0000	007D FFFF
131		007F 8000	007F 9FFF	:	:	:	:
130		007F 6000	007F 7FFF	8	64KB	0001 0000	0001 FFFF
129		007F 4000	007F 5FFF	7	8KB	0000 E000	0000 FFFF
128		007F 2000	007F 3FFF	6		0000 C000	0000 DFFF
127		007F 0000	007F 1FFF	5		0000 A000	0000 BFFF
126	64KB	007E 0000	007E FFFF	4		0000 8000	0000 9FFF
:	:	:	:	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 4. 64Mb Memory Map – x16 Top and Bottom Boot [134:0]

Block	Block Size	Address Range (x16 Top Boot)		Block	Block Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
134	4KW	003F F000	003F FFFF	134	32KW	003F 8000	003F FFFF
133		003F E000	003F EFFF	133		003F 0000	003F 7FFF
132		003F D000	003F DFFF	132		003E 8000	003E FFFF
131		003F C000	003F CFFF	:	:	:	:
130		003F B000	003F BFFF	8	32KW	0000 8000	0000 FFFF
129		003F A000	003F AFFF	7	4KW	0000 7000	0000 7FFF
128		003F 9000	003F 9FFF	6		0000 6000	0000 6FFF
127		003F 8000	003F 8FFF	5		0000 5000	0000 5FFF
126	32KW	003F 7000	003F 7FFF	4		0000 4000	0000 4FFF
:	:	:	:	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

Table 5. 64Mb Memory Map – x8/x16 Uniform Blocks [127:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
127	64KB	07F 0000h	07F FFFFh	127	32KW	03F 8000h	03F FFFFh
:		:	:	:		:	:
63		03F 0000h	03F FFFFh	63		01F 8000h	01F FFFFh
:		:	:	:		:	:
0		000 0000h	000 FFFFh	0		000 0000h	0000 7FFFh

Table 6. 32Mb Memory Map – x8 Top and Bottom Boot [70:0]

Block	Block Size	Address Range (x8 Top Boot)		Block	Block Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
70	8KB	003F E000	003F FFFF	70	64KB	003F 0000	003F FFFF
69		003F C000	003F DFFF	69		003E 0000	003E FFFF
68		003F A000	003F BFFF	68		003D 0000	003D FFFF
67		003F 8000	003F 9FFF	:	:	:	:
66		003F 6000	003F 7FFF	8	64KB	0001 0000	0001 FFFF
65		003F 4000	003F 5FFF	7	8KB	0000 E000	0000 FFFF
64		003F 2000	003F 3FFF	6		0000 C000	0000 DFFF
63		003F 0000	003F 1FFF	5		0000 A000	0000 BFFF
62	64KB	003E 0000	003E 1FFF	4		0000 8000	0000 9FFF
:	:	:	:	3		0000 6000	0000 7FFF
2	64KB	0002 0000	0002 FFFF	2		0000 4000	0000 5FFF
1		0001 0000	0001 FFFF	1		0000 2000	0000 3FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 1FFF

Table 7. 32Mb Memory Map – x16 Top and Bottom Boot [70:0]

Block	Block Size	Address Range (x16 Top Boot)		Block	Block Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
134	4KW	001F F000	001F FFFF	134	32KW	001F 8000	001F FFFF
133		001F E000	001F EFFF	133		001F 0000	001F 7FFF
132		001F D000	001F DFFF	132		001E 8000	001E FFFF
131		001F C000	001F CFFF	:	:	:	:
130		001F B000	001F BFFF	8	32KW	0000 8000	0000 FFFF
129		001F A000	001F AFFF	7	4KW	0000 7000	0000 7FFF
128		001F 9000	001F 9FFF	6		0000 6000	0000 6FFF
127		001F 8000	001F 8FFF	5		0000 5000	0000 5FFF
126	32KW	001F 7000	001F 7FFF	4		0000 4000	0000 4FFF
:	:	:	:	3		0000 3000	0000 3FFF
2	32KW	0001 0000	0001 7FFF	2		0000 2000	0000 2FFF
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

Table 8. 32Mb Memory Map – x8/x16 Uniform Blocks [63:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
63		03F 0000h	03F FFFFh	63		01F 8000h	01F FFFFh
:		:	:	:		:	:
0		000 0000h	000 FFFFh	0		000 0000h	0000 7FFFh

Table 9. 16Mb Memory Map – x8 Top/Bottom Boot [37:0]

Block	Block Size	Address Range (x8 Top Boot)		Block	Block Size	Address Range (x8 Bottom Boot)	
		Start	End			Start	End
37	8KB	001F E000	001F FFFF	37	64KB	001F 0000	001F FFFF
36		001F C000	001F DFFF	36		001E C000	001E FFFF
:		:	:	:		:	:
31		001F 0000	001F 1FFF	8		0001 0000	0001 FFFF
30	64KB	001E 0000	001E FFFF	7	8KB	0000 E000	0000 FFFF
:		:	:	:		:	:
1		0001 0000	0001 FFFF	1		0000 2000	0000 1FFF
0		0000 0000	0000 FFFF	0		0000 0000	0000 0FFF

Table 10. 16Mb Memory Map – x16 Top /Bottom Boot, Blocks [37:0]

Block	Block Size	Address Range (x16 Top Boot)		Block	Block Size	Address Range (x16 Bottom Boot)	
		Start	End			Start	End
37	4KW	000F F000	000F FFFF	37	32KW	000F 8000	000F FFFF
36		000F E000	000F EFFF	36		000F 0000	000F 7FFF
:		:	:	:		:	:
31		000F 8000	000F 8FFF	8		0000 8000	0000 FFFF
30	32KW	000F 0000	000F 7FFF	7	4KW	0000 7000	0000 7FFF
:		:	:	:		:	:
1		0000 8000	0000 FFFF	1		0000 1000	0000 1FFF
0		0000 0000	0000 7FFF	0		0000 0000	0000 0FFF

Table 11. 16Mb Memory Map – x8/x16 Uniform Blocks [31:0]

Block	Block Size	Address Range (x8)		Block	Block Size	Address Range (x16)	
		Start	End			Start	End
31	64KB	01F 0000h	01F FFFF	31	32KW	00F 8000h	00F FFFFh
:		:	:	:		:	:
0		000 0000	000 FFFF	0		000 0000	000 7FFF

BUS Operations

Table 12. Device OPERATING MODES

Operation	CE#	OE#	WE#	RST#	Vpp/WP#	x8 Mode			X16 Mode	
						A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Byte address	High-Z	Data output	Word address	Data output
WRITE	L	H	L	H	H(3)	Command address	High-Z	Data input(4)	Command address	Data input(4)
STANDBY	H	X	X	H	H	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitch of less than 3ns on CE#, WE#, and RESET# are ignored by the device and do not affect bus operation.
2. H = Logic level HIGH (VIH); L = Logic Level LOW (VIL); X = HIGH or LOW
3. If WP# is LOW, then the highest or lowest block remains protected, or the top two blocks or the bottom two blocks, depending on the item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 8 words (16 bytes) and is addressed by address inputs A [2:0] in x16 bus mode and A[2:0] plus DQ15/A-1 in x8 bus mode. The extended memory blocks and CFI area do not support page mode.

A valid bus READ operations involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value.

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE$ or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation.

Standby

During CE# HIGH in read mode causes the device to enter standby, and data I/O to be High-Z. To reduce the supply current to the standby supply current, CE# must held within Vcc +/-0.3V.
During PROGRAM or ERASE operations, the device will continue to use the program/erase supply current (Icc3) until the operation completes.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for tACC + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system.

Output Disable

Data I/O are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to standby level, independently from CE#, OE#, or WE# inputs.

Registers

Status Register

Table 13. Status Register Bit Definitions

Bit	Name	Setting	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 3, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program/erase controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors the program/erase controller during ERASE operations. During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, wtht each successive READ operation from addresses within the blocks being erased.	3, 4, 7
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode.	

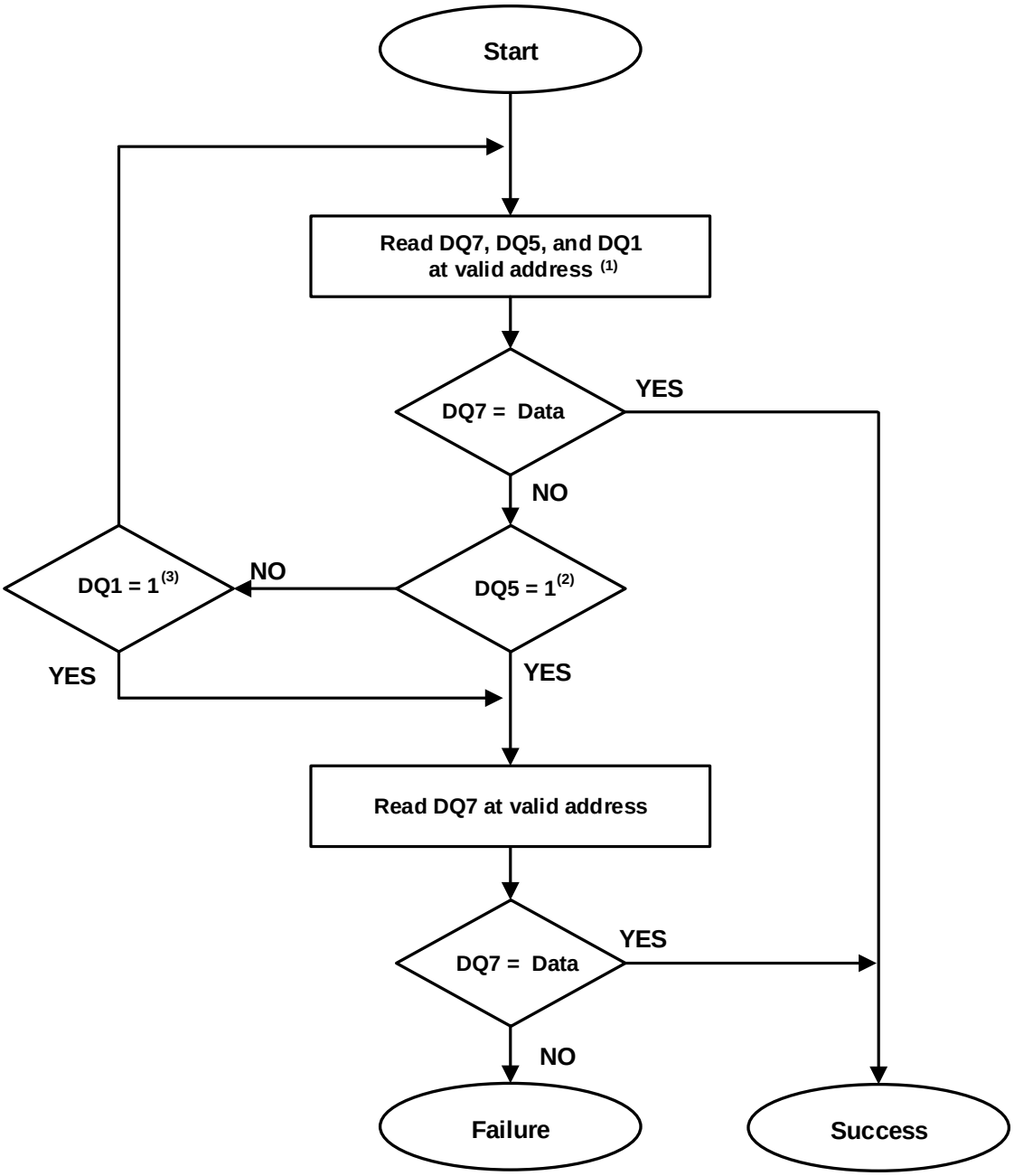
Notes:
1. The status register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ [7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE or BLANK CHECK operation in progress, DQ7 outputs 0; upon either operation's successful completion, DQ7 outputs 1.
3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During erase suspend mode, READ operations to address within blocks not being erased output memory array .data as if in read mode. A protected block is treated the same as a block not being erased.
5 During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation.
6 When DQ5 is set to 1, a READ/RESET command must be issued before any subsequent command.
7. DQ2 toggles for an actively erasing block during BLOCK ERASE operation.

Table 14. Operations and Corresponding Bit Settings

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	-	-	0	0	2
BLANK CHECK	Any address	0	Toggle	0	-	-	0	0	
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	-	0	
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	-	0	
	Non-erasing block	0	Toggle	0	0	No Toggle	-	0	
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	-	0	3
	Non-erasing block	0	Toggle	0	1	No Toggle	-	0	
PROGRAM SUSPEND	Programming block	Invalid operation						High-Z	
	Non-programming block	Outputs memory array data as if in read mode						High-Z	
ERASE SUSPEND	Erasing blk	1	No Toggle	0	-	Toggle	-	High-Z	
	Non-erasing blk	Outputs memory array data as if in read mode						High-Z	
PROGRAM during ERASE SUSPEND	Erasing block	DQ7#	Toggle	0	-	Toggle	-	0	2
	Non-erasing block	DQ7#	Toggle	0	-	No Toggle	-	0	2
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	-	-	1	0	
PROGRAM Error	Any address	DQ7#	Toggle	1	-	-	-	0	2
ERASE Error	Erase success block	0	Toggle	1	1	No Toggle	-	0	
	Erase fail block	0	Toggle	1	1	Toggle	-	0	
BLANK CHECK Error	Any address	0	Toggle	1	1	Toggle	-	0	

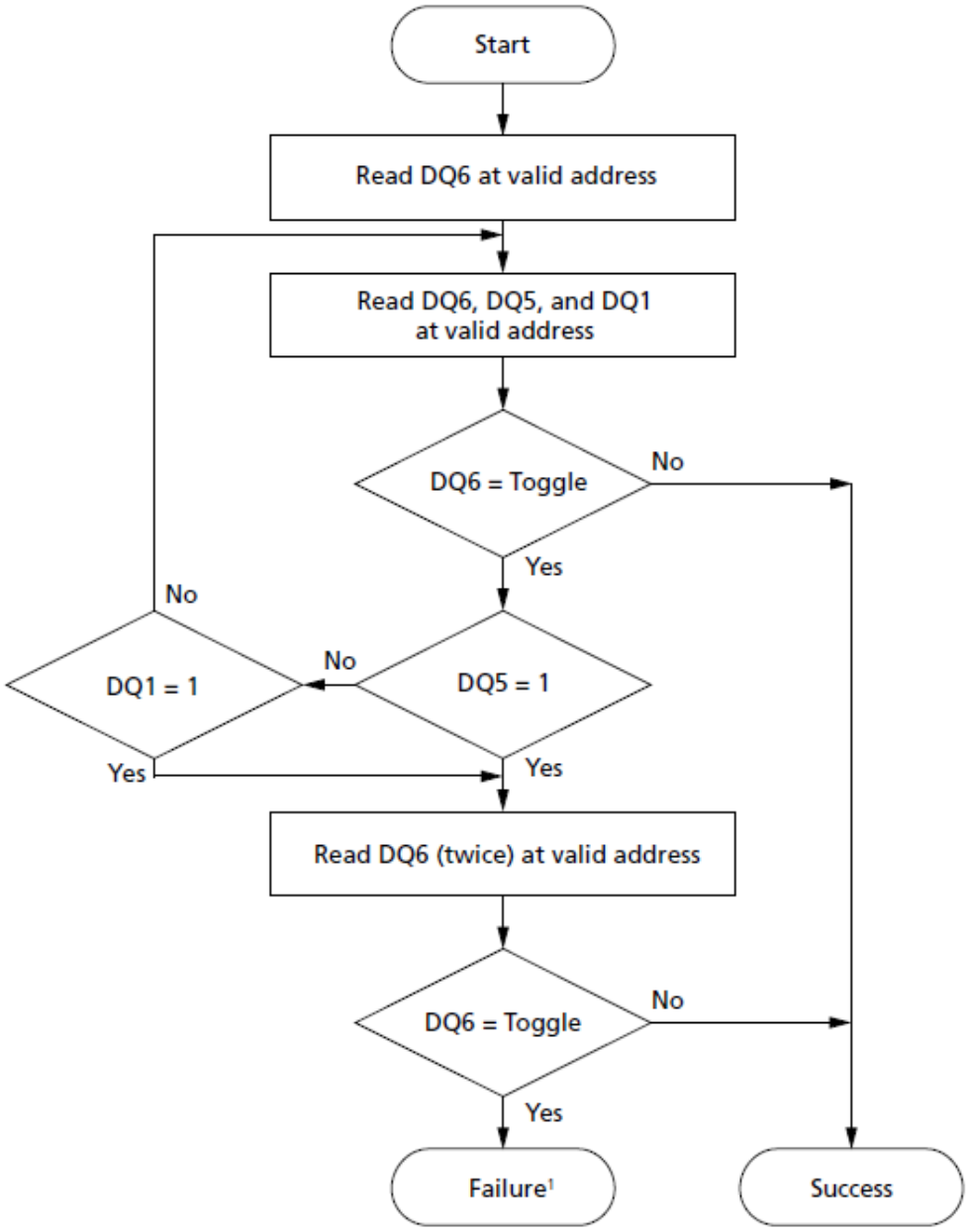
Notes:
1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.
3. DQ2 toggles only for actively erasing block during BLOCK ERASE operation.

Figure 7. Data Polling Flowchart



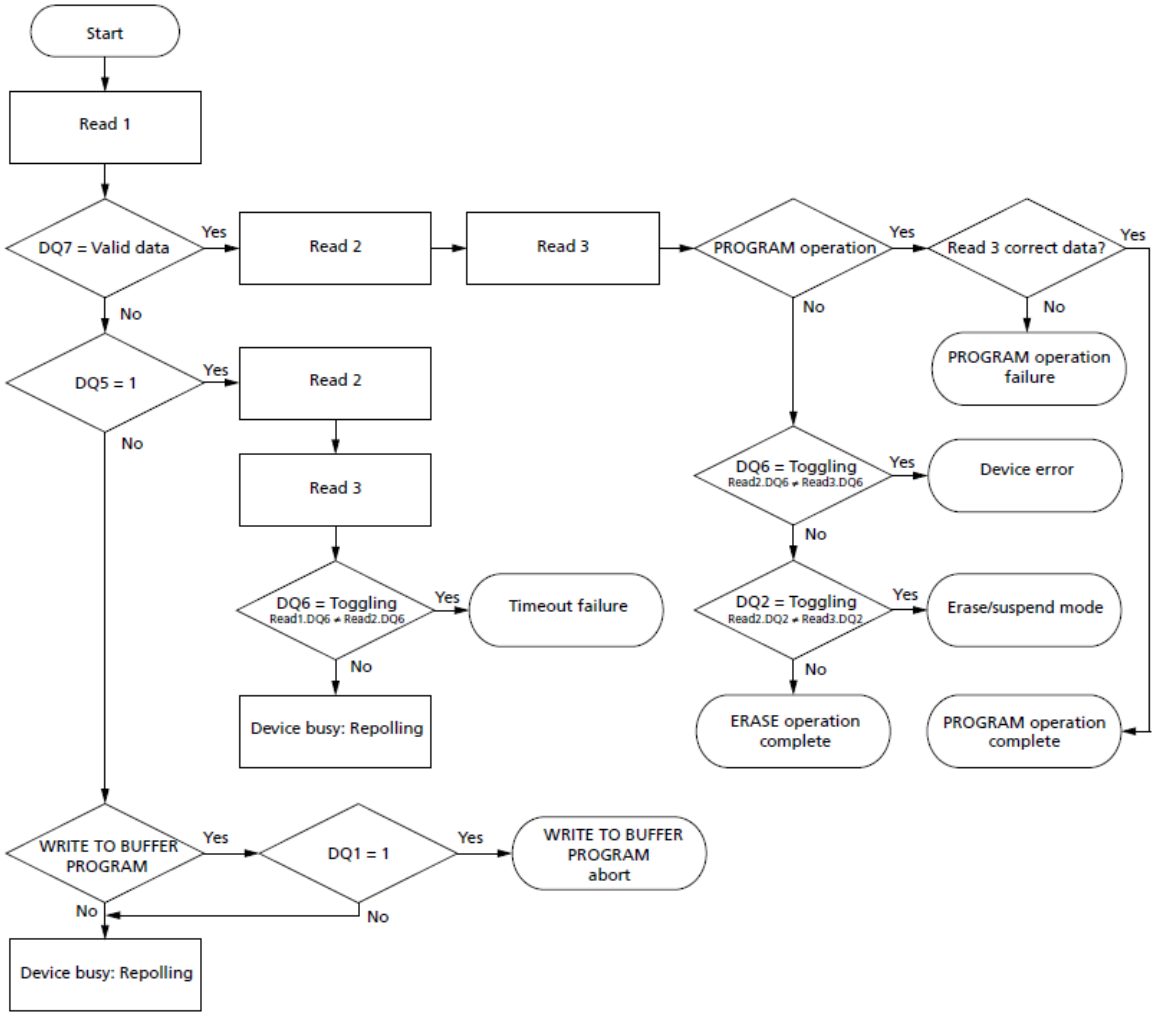
Notes:
1. Valid address is the address being programmed or an address within the block being erased.
2. Failure results: DQ5 = 1 indicates an operation error.
3. DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 8. Toggle Bit Flowchart



Note:
1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.

Figure 9. Status Register Polling Flowchart



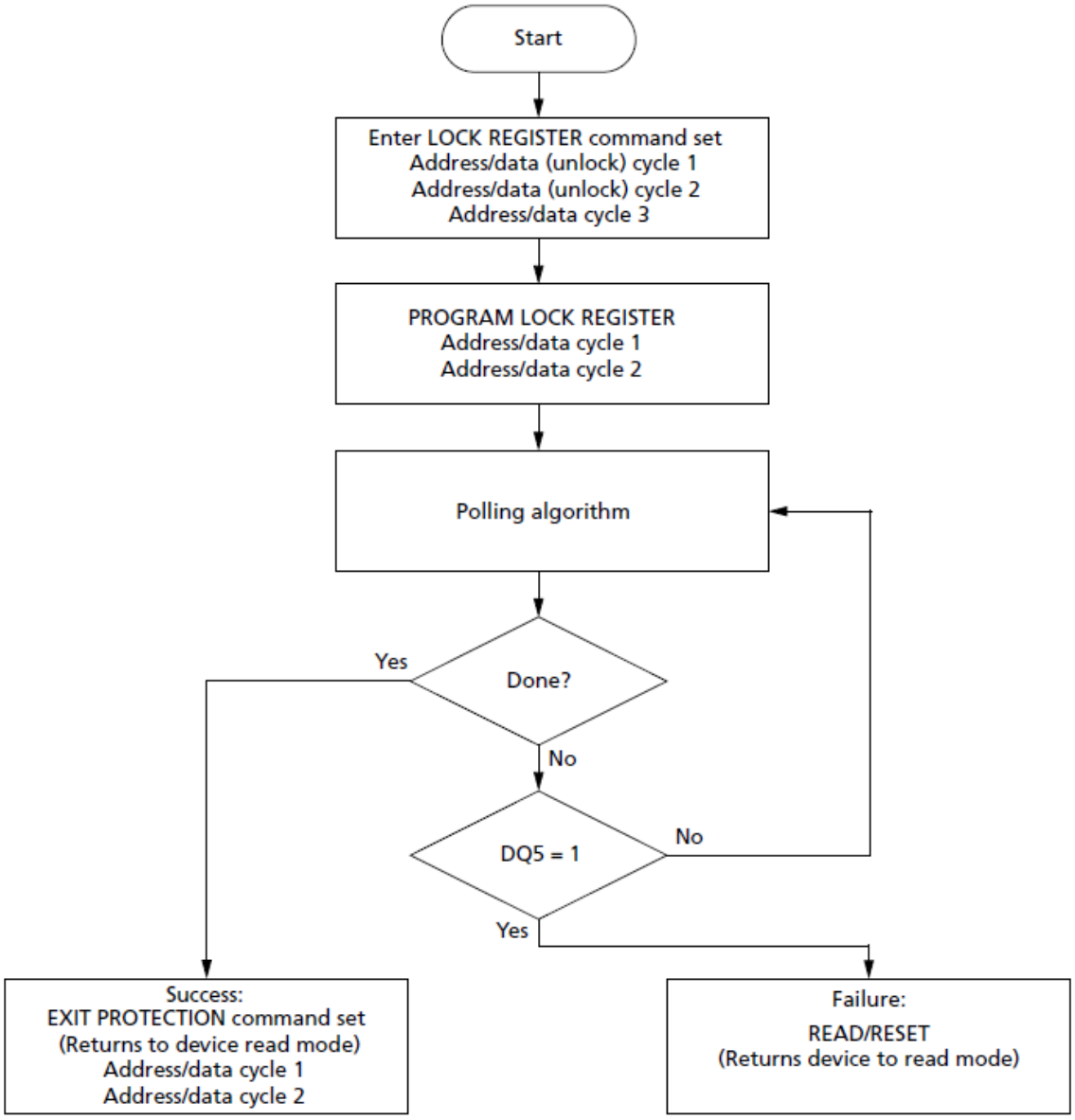
Lock Register

Table 15. Lock Register Bit Definitions

Bit	Name	Settings	Description	Notes
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	

Notes:
1. The lock register is a 16-bit, one time programmable register. DQ [15:3] are reserved and are set to a default value of 1.
2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Figure 10. Lock Register Program Flowchart



Notes:

1. Each lock register bit can be programmed only one.

Standard Command Definitions – Address Data Cycles

Table 16. Standard Command Definitions – Address-Data Cycles, x8 and x16

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	X8	X	F0											
		AAA	AA	555	55	X	F0							
	X16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	X8	AA	98											
	X16	55												
AUTO SELECT (90h)	X8	AAA	AA	555	55	AAA	90	Note 2	Note 2					2,3,4
	X16	555		2AA		555								
BYPASS Operations														
UNLOCK BYPASS (20h)	X8	AAA	AA	555	55	AAA	20							
	X16	555		2AA		555								
UNLOCK BYPASS RESET (90h/00h)	X8	X	90	X	00									
	X16													
PROGRAM Operations														
PROGRAM (A0h)	X8	AAA	AA	555	55	AAA	A0	PA	PD					
	X16	555		2AA		555								
UNLOCK BYPASS PROGRAM (A0h)	X8	X	A0	PA	PD									5
	X16													
DOUBLE BYTE/WORD PROGRAM (50h)	X8	AAA	50	PA2	PD									
	X16	555												
QUADRUPLE BYTE/WORD PROGRAM (56h)	X8	AAA	56	PA4	PD									
	X16	555												
OCTUPLE BYTE PROGRAM (8Bh)	X8	AAA	8B	PA8	PD									6

Table 16. Standard Command Definitions – Address-Data Cycles, x8 and x16 (Continued)

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
WRITE TO BUFFER PROGRAM (25h)	X8	AAA	AA	555	55	BAd	25	BAd	N	PA	PD			7, 8, 9
	X16	555		2AA										
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	X8	BAd	25	BAd	N	PA	PD							5
	X16													
WRITE TO BUFFER PROGRAM CONFIRM (29h)	X8	BAd	29											
	X16													
BUFFERED PROGRAM ABORT and RESET (F0h)	X8	AAA	AA	555	55	AAA	F0							
	X16	555		2AA		555								
PROGRAM SUSPEND (B0h)	X8	X	B0											
	X16													
PROGRAM RESUME (30h)	X8	X	30											
	X16													
ERASE Operations														
CHIP ERASE (80/10h)	X8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10	
	X16	555		2AA		555		555		2AA		555		
UNLOCK BYPASS CHIP ERASE (80/10h)	X8	X	80	X	10									5
	X16													
BLOCK ERASE (80/30h)	X8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30	10
	X16	555		2AA		555		555		2AA				
UNLOCK BYPASS BLOCK ERASE (80/30h)	X8	X	80	BAd	30									5
	X16													
ERASE SUSPEND (B0h)	X8	X	B0											
	X16													
ERASE RESUME (30h)	X8	X	30											
	X16													

Table 16. Standard Command Definitions – Address-Data Cycles, x8 and x16 (Continued)

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
BLANK CHECK Operations														
BLANK CHECK SETUP (EB/76h)	X8	AAA	AA	555	55	BAd	EB	BAd	76	BAd	00	BAd	00	
	X16	555		2AA										
BLANK CHECK CONFIRM and READ (29h)	X8	BAd	29	BAd	Note 2									2
	X16													

Notes:

1. A = Address; D = Data; X = Don't Care, BAd = Any address in the block; N = Number of bytes to be programmed; PA = program address; PA2 = Program address with constant AMAX:A0 for x8 or AMAX:A1 for x16, which should be used two times to select adjacent two bytes/words; PA4 = Program address with constant AMAX:A1 for x8 or AMAX:A2 for x16, which should be used four times to select four bytes/words; PA8 = Program address with constant AMAX:A2 for x8, which should be used eight times to select adjacent eight bytes; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
2. These cells represent READ cycles (versus WRITE cycles for others).
3. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
4. AUTO SELECT addresses and data are specified in the Electronic Signature table and the extended Memory Block Protection table.
5. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
6. This command is only for x8 devices.
7. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
8. WRITE TO BUFFER PROGRAM operation: maximum cycles = 261 (x8) and 261 (x16).
   UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 259 (x8), 259 (x16).
   WRITE TO BUFFER PROGRAM operation: N +1 = bytes to be programmed;
   Maximum buffer size = 256 bytes (x8) and 512 bytes (x16)
9. For x8, A [MAX: 7] address pins should remain unchanged while A [6:0] and A-1 pins are used to select a byte within the N+1 byte page. For x16, A [MAX: 8] address pins should remain unchanged while A [7:0] pins are used to select a word within the N+1 word page.
10. BLLOCK ERASE address cycles can extend beyond size address data cycles, depending on the number of blocks to erase.

READ and AUTO SELECT Operations

READ/RESET Command

The READ/RESET (F0h) command returns the device to read mode and resets the errors in the status register. One or three bus WRITE operations can be used to issue the READ/RESET command.

To return te device to read mode, this command can be issued between bus WRITE cycles before the start of a PROGRAM or ERASE operation. If the READ/RESET command is issued during the timeout of a BLOCK ERASE operation, the device requires up to 10us to abort, during which time no valid data can be read.

This command will not abort an ERASE operation while in erase suspend.

READ CFI Command

The READ CFI (98h) command puts the device in read CFI mode and is only valid when the device is in read array or auto select mode. One bus WRITE cycle is required to issue the command.

Once in read CFI mode, bus READ operations will output data from the CFI memory area. A READ/RESET command (F0h) must be issued to return the device to the previous mode (read array or auto select). A second READ/RESET command is required to put the device in read array mode from auto select mode.

Auto Select command

At power-up or after a hardware reset, the device is in read mode. Then it can be put in auto select mode by issuing an AUTO SELECT (90h) command.

The Auto Select mode provides;

- Electronic signature, which includes manufacturer ID, Device identification as shown in Electronic Signature table.
- Block protection information, which includes the block protection status and extended memory block protection indicator.

Electronic signature or block protection information is read by executing a READ operation with control signals and addresses set. In addition, this device information can be read or set by issuing an AUTO SELECT command.

- Auto select mode can be used by programming equipment to automatically match a device with the application code to be programmed.
- Three consecutive bus WRITE operations are required to issue an AUTO SELECT command. The device remains in auto select mode until a READ/RESET or READ CFI command is issued.
- The device cannot enter auto select mode when a PROGRAM or ERASE operation is in progress (RY/BY# LOW). However, the device can enter auto select mode if Programming or Erase operation has been suspended by issuing a PROGRAM SUSPEND or ERASE SUSPEND command.
- When Auto select mode is exited by performing a reset. The device returns to read mode unless it entered auto select mode after an ERASE SUSPEND or PROGRAM SUSPEND command, in which case it returns to erase or program suspend mode.

Table 18. Read Electronic Signature

Read Cycle		CE#	OE#	WE#	Address Input							Data Input/Output		
					X8/x16						x8 only	X8 only		x16 only
					A[MAX:11]	A[10:4]	A3	A2	A1	A0	A-1	DQ[14:8]	DQ[7:0]	DQ[15:0]
Manufacturer code		L	L	H	X	L	L	L	L	L	X	X	9Dh	009Dh
Device ID 1		L	L	H	X	L	L	L	L	H	X	X	7Eh	227Eh
Device ID 2	64Mb boot	L	L	H	X	L	H	H	H	L	X	X	10h	2210h
	64Mb uniform												0Ch	220Ch
	32Mb boot												1Ah	221Ah
	32Mb uniform												1Dh	221Dh
	16Mb boot												C4h	22C4h
	16Mb uniform												49h	2249h
Device ID 3	64Mb uniform	L	L	H	X	L	H	H	H	H	X	X	01h	2201h
	64Mb top													
	32Mb top													
	16Mb top													
Device ID 3	64Mb bottom	L	L	H	X	L	H	H	H	H	X	X	00h	2200h
	32Mb bottom													
	16Mb bottom													
	32Mb uniform													
	16Mb uniform													

Note:

1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.

Table 19. Block Protection

Read Cycle		CE#	OE#	WE#	Address Input						Data Input/Output		
					X8/x16					x8 only	X8 only		x16 only
	Option (6)				A[MAX:15]	A[14:11]	A[10:2]	A1	A0	A-1	DQ[14:8]	DQ[7:0]	DQ[15:0]
Extended memory Block protection indicator (DQ7)	L	L	L	H	X	X	L	H	H	X	X	8Ah(2)	008Ah(2)
												0Ah(3)	000Ah(3)
	H	L	L	H	X	X	L	H	H	X	X	9Ah(2)	009Ah(2)
												1Ah(3)	001Ah(3)
	B	L	L	H	X	X	L	H	H	X	X	8Ah(2)	008Ah(2)
												0Ah(3)	000Ah(3)
	T	L	L	H	X	X	L	H	H	X	X	9Ah(2)	009Ah(2)
												1Ah(3)	001Ah(3)
Block Protection staus		L	L	H	Block base address	L	L	H	L	X	X	01h(4)	0001h(4)
												00h(5)	0000h(5)

Notes:
1. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
2. ISSI – prelocked (permanent).
3. Customer lockable.
4. Protected: 01h (in x8 mode) is output on DQ [7:0].
5. Unprotected: 00h (in x8 mode) is output on DQ [7:0].
6. Block Protection Option:
   H = Highest block protected by Vpp/WP#; uniform block
   L = Lowest block protected by Vpp/WP#; uniform block
   T = Top boot; top two blocks protected by Vpp/WP#
   B = Bottom boot; bottom two blocks protected by Vpp/WP#

Bypass Operations

UNLOCK BYPASS Command

The UNLOCK BYPASS (20h) command is used to place the device in unlock bypass mode. Three bus WRITE operations are required to issue the UNLOCK BYPASS command.

When the device enters unlock bypass mode, the two initial UNLOCK cycles required for a standard PROGRAM or ERASE operation are not needed, thus enabling faster total program or erase time.

The UNLOCK BYPASS command is used in conjunction with UNLOCK BYPASS PROGRAM or UNLOCK BYPASS ERASE commands to program or erase the device faster than with standard PROGRAM or ERASE commands. Using these commands can save considerable time when the cycle time to the device is long. When in unlock bypass mode, only following commands are valid:

- The UNLOCK BYPASS PROGRAM command can be issued to program addresses within the device.
- The UNLOCK BYPASS ERASE command can be issued to erase one or more memory blocks.
- The UNLOCK BYPASS CHIP ERASE command can be issued to erase the whole memory array.
- The UNLOCK BYPASS RESET command can be issued to return the device to read mode.

Also the device can enter UNLOCK BYPASS mode when Vpp/WP# is raised to V_{PPH}.
When Vpp/WP# returns to V_{IH} or V_{IL}, the device is no longer in unlock bypass mode, and normal operation resumes.

The transition from V_{IH} to V_{PPH} and from VPPH to V_{IH} must be slower than tVHVPP.

Note: It is recommended that entering and exiting unlock bypass mode using the ENTER UNLOCK BYPASS and UNLOCK BYPASS RESET commands rather than raising Vpp/WP# to V_{PPH}.
Vpp/WP# should never be raised to V_{PPH} from any mode except read mode; otherwise, the device may be left in an indeterminate state.

UNLOCK BYPASS RESET Command

The UNLOCK BYPASS RESET (90/00h) command is used to return to read/reset mode from unlock bypass mode. Two bus WRITE operations are required to issue the UNLOCK BYPASS RESET command. The READ/RESET command does not exit from unlock bypass mode.

Program Operations

The PROGRAM (A0h) command is used to program a value to address in the memory array.

The command requires 4 bus WRITE operations, and the final WRITE operation latches the address and data in the internal state machine and starts the program/erase controller. After programming has started, bus READ operations output the status register content.

Programming can be suspended and then resumed by issuing a PROGRAM SUSPEND command and a PROGRAM RESEUM command, respectively.

If programming address is within a protected block, the PROGRAM command is ignored, and the data remains unchanged. The status register is not read, and no error condition is given.

After the PROGRAM operation has completed, the device returns to read mode, unless an error has occurred.

When an error occurs, bus READ operations to the device continue to output the status register.
A READ/RESET command must be issued to reset the error condition and return the device to read mode.

The PROGRAM command cannot change a bit set to 0 back to 1, and an attempt to do so is masked during a PROGRAM operation. Instead, an ERASE command must be used to set all bits in one memory block or in the entire memory from 0 to 1.

The PROGRAM operation is aborted by performing a hardware reset or by powering-down the device. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

UNLOCK BYPASS PROGRAM Operations

When the device is in unlock bypass mode, the UNLOCK BYPASS PROGRAM (A0h) command can be used to program one address in the memory array. The command requires two bus WRITE operations instead of four, which is required by a standard PROGRAM command; the final WRITE operation latches the address and data and starts the program/erase controller. The PROGRAM operation using the UNLOCK BYPASS PROGRAM command behaves identically to the PROGRAM operation using the PROGRAM command. The operation cannot be aborted.
A bus READ operation to the memory outputs the status register.

DOUBLE BYTE/WORD PROGRAM Command

The DOUBLE BYTE/WORD PROGRAM (50h) command is used to write a page of two adjacent bytes/words in parallel. The two bytes/words must differ only for the address A-1 or A0, respectively.
Three bus write cycles are necessary to issue the command:

- The first bus cycle sets up the command.
- The second bus cycle latches the address and data of the first byte/word to be programmed.
- The third bus cycle latches the address and data of the second byte/word to be programmed and starts the program/erase controller.

Note: The DOUBLE BYTE/WORD PROGRAM command is available only in the 32Mb and 64Mb devices; also only V_{PPL} is to be applied to the Vpp/WP# pin.

QUADRUPLE BYTE/WORD PROGRAM Command

The QUADRUPLE BYTE/WORD PROGRAM (56h) command is used to write a page of four adjacent bytes/words in parallel. The four bytes/words must differ only for the address A0, DQ15/A-1 in x8 mode or for addresses A1, A0 in x16 mode.
Five bus write cycles are necessary to issue the command:

- The first bus cycle sets up the command.
- The second bus cycle latches the address and data of the first byte/word to be programmed.
- The third bus cycle latches the address and data of the second byte/word to be programmed.
- The fourth bus cycle latches the address and data of the third byte/word to be programmed.
- The fifth bus cycle latches the address and data of the fourth byte/word to be programmed and starts the program/erase controller.

Note: The QUADRUPLE BYTE/WORD PROGRAM command is available only in the 32Mb and 64Mb devices; also only V_{PPL} is to be applied to the Vpp/WP# pin.

OCTUPLE BYTE PROGRAM Command

The OCTUPLE BYTE PROGRAM (8Bh) command is used to write a page of eight adjacent bytes in parallel. The eight bytes must differ only for the address A1, A0, DQ15/A-1 in x8 mode only.

Nine bus write cycles are necessary to issue the command:
The first bus cycle sets up the command.
The second bus cycle latches the address and data of the first byte to be programmed.
The third bus cycle latches the address and data of the second byte to be programmed.
The fourth bus cycle latches the address and data of the third byte to be programmed.
The fifth bus cycle latches the address and data of the fourth byte to be programmed.
The sixth bus cycle latches the address and data of the fifth byte to be programmed.
The seventh bus cycle latches the address and data of the sixth byte to be programmed.
The eighth bus cycle latches the address and data of the seventh byte to be programmed.
The ninth bus cycle latches the address and data of the eighth byte to be programmed and starts the program/erase controller.

Note: The OCTUPLE BYTE PROGRAM command is available only in the 32Mb and 64Mb X8 devices; also only V_{PPL} is to be applied to the Vpp/WP# pin.

WRITE TO Buffer PROGRAM Command

The WRITE TO BUFFER PROGRAM (25h) command makes use of the program buffer to speed up programming and dramatically reduces system programming time compared to standard non-buffered PROGRAM command.

Maximum program buffer size is 256 words.

When issuing a WRITE TO BUFFER PROGRAM command, Vpp/WP# can be held HIGH or raised to V_{PPH}. Also, it can be held LOW if the block is not the lowest or highest block or the top/bottom two blocks, depending on the part number. When VPPH is applied to the Vpp/WP# pin during execution of the command, programming speed increases.

The following steps are required to issue the WRITE TO BUFFER PROGRAM command:

- Two UNLOCK cycles are issued.
- A third bus WRITE cycle sets up the WRITE TO BUFFER PROGRAM command. The set-up code can be addressed to any location within the targeted block.
- A fourth bus WRITE cycle sets up the number of words/bytes to be programmed. Value n is written to the same block address, where n+1 is the number of words/bytes to be programmed. Value n+1 must not exceed the size of the program buffer, or the operation will abort.
- A fifth cycle loads the first address and data to be programmed.
- Last, n bus WRITE cycles load the address and data for each word/bytes into the program buffer. Addresses must lie within the range from the ***start address+1*** to the ***start address + (n-1)***.

Optimum programming performance and lower power usage are achieved by aligning the starting address at the beginning of a 256-word boundary (A [7:0] = 0x000h). Any buffer size smaller than 256 word is allowed within a 256-word boundary, while all addresses used in the operation must lie within the 256-word boundary. In addition, any crossing boundary buffer program will result in a program abort.
For x8 device, maximum buffer size is 256 bytes; for x16 device, maximum buffer size is 512 bytes.

To program the content of the program buffer, this command must be followed by a WRITE TO BUFFER PROGRAM CONFIRM command.

If an address is written several times during a WRITE TO BUFFER PROGRAM operation, the address/data counter will be decremented at each data load operation, and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or the incorrect sequence of the bus WRITE cycles will abort the WRITE TO BUFFER PROGRAM command.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a WRITE TO BUFFER PROGRAM operation.

The WRITE TO BUFFER PROGRAM command should not be used to change a bit set to 0 back to 1, and an attempt to do so is masked during the operation. Rather than the WRITE TO BUFFER PROGRAM command, the ERASE command should be used to set memory bits from 0 to 1.

Figure 11. Boundary Condition of Program Buffer Size

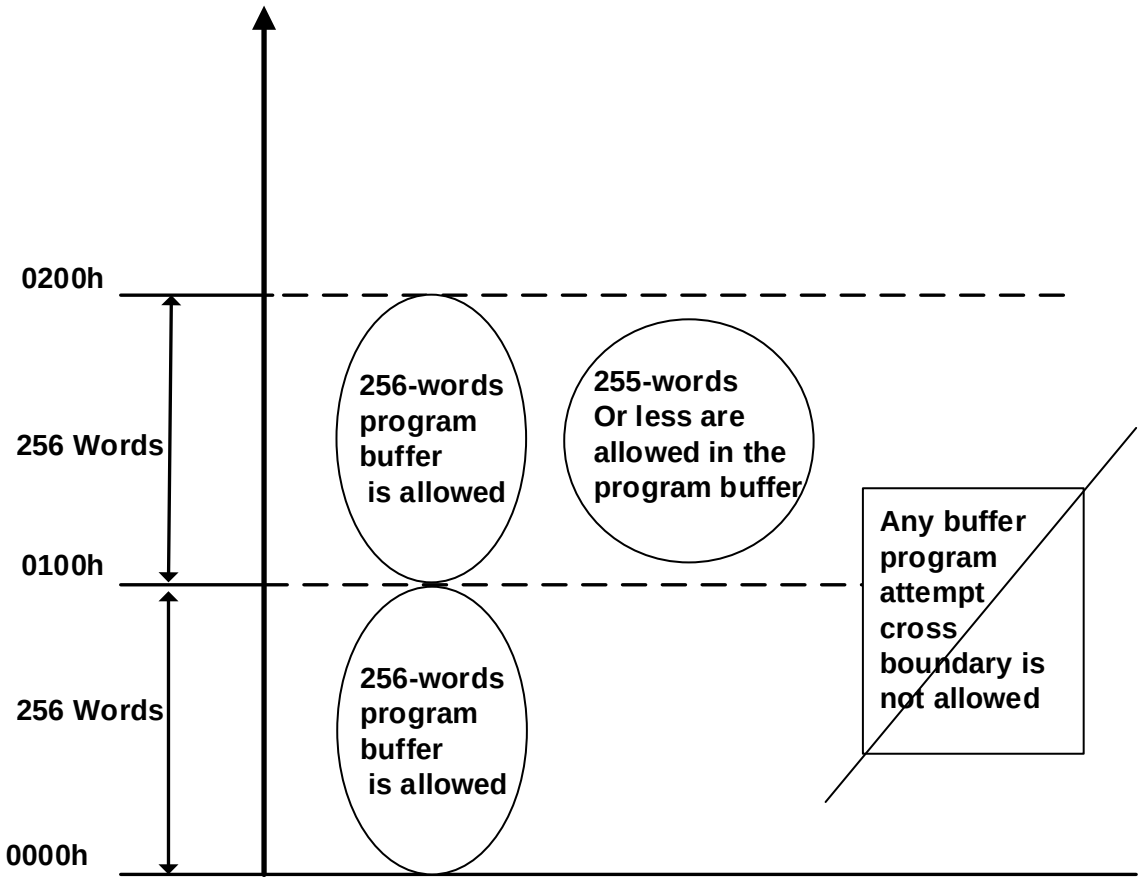
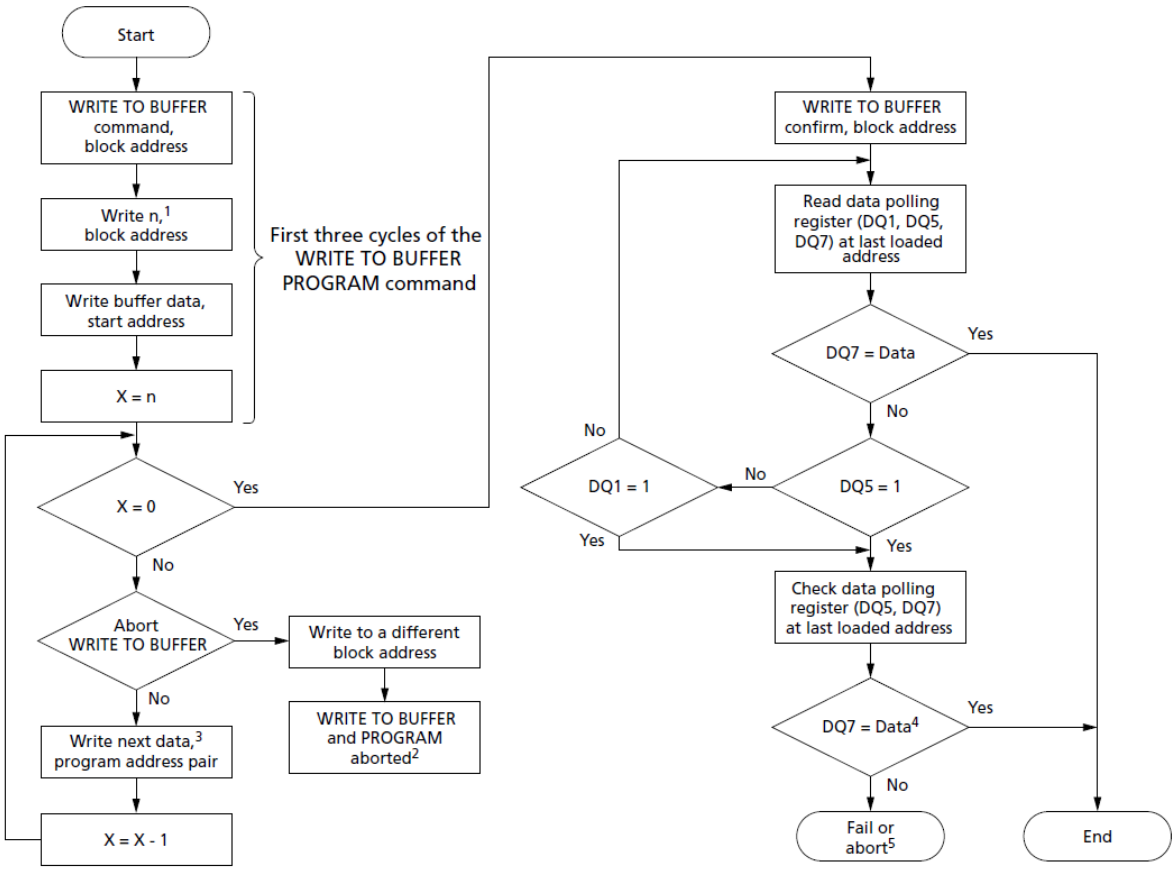


Figure 12. WRITE TO BUFFER PROGRAM Flowchart



Notes:

1. N+1 is the number of addresses to be programmed.
2. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However, when loading program buffer address with data, all addresses must fall within the selected program buffer page.
4. DQ7 must be checked because DQ5 and DQ7 may change simultaneously.
5. If this flowchart location is reached because DQ5=1, then the WRITE TO BUFFER PROGRAM command failed.
   If this flowchart location is reached because DQ1 = 1, then the WRITE TO BUFFER PROGRAM command aborted. In both cases, the appropriate RESET command must be issued to return the device to read mode:
   A RESET command if the operation failed; A WRITE TO BUFFER PROGRAM ABORT AND RESET command if the operation aborted.

UNLOCK BYPASS WRITE TO BUFFER PROGRAM Command

When the device is in unlock bypass mode, the UNLOCK BYPASS WRITE TO BUFFER PROGRAM command (25h) can be used to program the device in fast program mode. The command requires two bus WRITE operations fewer than the standard WRITE TO BUFFER PROGRAM command.

The UNLOCK BYPASS WRITE TO BUFFER PROGRAM command behaves the same way as the WRITE TO BUFFER PROGRAM command: the operation cannot be aborted, and a bus READ operation to the memory outputs the status register.

The WRITE TO BUFFER PROGRAM CONFIRM command is used to confirm an UNLOCK BYPASS WRITE TO BUFFER PROGRAM command and to program the n+1 words/bytes loaded in the program buffer by this command.

WRITE TO BUFFER PROGRAM CONFIRM Command

The WRITE TO BUFFER PROGRAM CONFIRM (29h) command is used to confirm a WRITE TO BUFFER PROGRAM command to program the n+1 words/bytes loaded in the program buffer by this command.

BUFFERED PROGRAM ABORT AND RESET Command

A BUFFERED PROGRAM ABORT AND RESET (F0h) command must be issued to reset the device to read mode when the BUFFER PROGRAM operation is aborted. The buffer programming sequence can be aborted in the following ways.

- Load a value that is greater than the page buffer size during the number of locations to program in the WRITE TO BUFFER PROGRAM command.
- Write to an address in a different block than the one specified during the WRITE BUFFER LOAD command.
- Write an address/data pair to a different write buffer page than the one selected by the starting address during the program buffer data loading stage of the operation.
- Write data other than the CONFIRM command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DQ7# (for the last address location loaded), DQ6 = toggle, DQ5 = 0 (all of which are status register bits).

A BUFFERED PROGRAM ABORT and RESET command sequence must be written to reset the device for the next operation.

Note: The full three-cycle BUFFERED PROGRAM ABORT and RESET command sequence is required when using buffer programming features in unlock bypass mode.

PROGRAM SUSPEND Command

The PROGRAM SUSPEND (B0h) command allows the system to interrupt a PROGRAM operation or a “Write to Buffer” programming operation so that data can be read from any non-suspended block. When the PROGRAM SUSPEND command is issued during a programming process, the device suspends the programming operation within the program suspend latency time **(15 µs maximum, 5 µs typical)** and updates the status register bits. Addresses are “don't-cares” when writing the Program Suspend command.

After the PROGRAM operation has been suspended, data can be read array data from any non-suspended block.

The PROGRAM SUSPEND command may also be issued during a PROGRAM operation while an erase is suspended. In this case, data may be read from any addresses not within a block in ERASE SUSPEND or PROGRAM SUSPEND.

If a read is needed from the extended memory block area (one-time programmable area), the ENTER/EXIT EXTENDED MEMORY BLOCK command sequence must be issued.

The system may also issue the AUTO SELECT command sequence and CFI query command when the device is in program suspend mode. The system can read as many auto select codes as required.

When the device exits the auto select mode, the device reverts to Program Suspend mode, and is ready for another valid operation.

The PROGRAM SUSPEND operation is aborted by performing a device reset or power down. In this case, data integrity cannot be ensured, and it is recommended that the words or bytes that were aborted be reprogrammed.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the write operation status bits, just as in the standard program operation.

PROGRAM RESUME command

The PROGRAM RESUME (30h) command must be issued to exit a program suspend mode and resume a PROGRAM operation. The host can use DQ7 or DQ6 status bits to determine the status of the PROGRAM operation. After a PROGRAM RESUME command is issued, subsequent PROGRAM RESUME commands are ignored. Another PROGRAM SUSPEND command can be issued after the device has resumed programming.

Erase Operations

CHIP ERASE Command

CHIP ERASE (80/10h) command erases the entire chip. Six bus WRITE operations are required to issue the command and start the program/erase controller.

Protected blocks are not erased. If all blocks are protected, the data remains unchanged.
No error is reported when protected blocks are not erased.

During the CHIP ERASE operation, the device ignores all other commands, including ERASE SUSPEND.
It is not possible to abort the operation. All bus READ operations during CHIP ERASE output the data polling register on the data I/Os.

After the CHIP ERASE operation completes, the device returns to read mode, unless an error has occurred. If an error occurs, the device will continue to output the data polling register.

When the operation fails, a READ/RESET command must be issued to reset the error condition and return to read mode. The status of the array must be confirmed through the BLANK CHECK operation and the BLOCK ERASE command re-issued to the failed block.

The CHIP ERASE command sets all of the bits in unprotected blocks of the device to 1. All previous data is lost.

The operation is aborted by performing a hardware reset or by powering down the device. In this case, data integrity cannot be ensured, and it is recommended that the entire chip should be erased again.

UNLOCK BYPASS CHIP ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS CHIP ERASE (80/10h) command can be used to erase all memory blocks at one time. The command requires only two bus WRITE operations instead of six using the standard CHIP ERASE command. The final bus WRITE operation starts the program/erase controller.

The UNLOCK BYPASS CHIP ERASE command behaves the same way as the CHIP ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the data polling register.

BLOCK ERASE command

The BLOCK ERASE (80/30h) command erases a list of one or more blocks. It sets all bits in the selected, unprotected blocks to 1. All previous, selected, unprotected blocks data in the selected blocks is lost.

Six bus WRITE operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth bus WRITE operation using the address of the additional block. After the command sequence is written, a block erase timeout occurs.

During the period specified by the block erase timeout parameter, additional block addresses and BLOCK ERASE commands can be written. Any command except BLOCK ERASE or BLCOK SUSPEND during this timeout period resets that block to the read mode. The system can monitor DQ3 to determine if the block erase timer has timed out.

After the program/erase controller has started, it is not possible to select any more blocks. Each additional block must therefore be selected within the timeout period of the last block. The timeout timer restarts when an additional block is selected. After the sixth bus WRITE operation, a bus READ operation outputs the data polling register. A READ/RESET command must be issued to reset the error condition and return to read mode.

If any selected blocks are protected, they are ignored, and all other selected blocks are erased. If all selected blocks are protected, the data remains unchanged. No error condition is given when protected blocks are not erased.

During the BLOCK ERASE operation, the device ignores all commands except the ERASE SUSPEND command and the READ/RESET command, which is accepted only during the timeout period. The operation is aborted by performing a hardware reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended that the aborted blocks be erased again.

UNLOCK BYPASS BLOCK ERASE Command

When the device is in unlock bypass mode, the UNLOCK BYPASS BLCOK ERASE (80/30h) command can be used to erase one or more memory blocks at a time. The command requires only two bus WRITE operations instead of six using the standard BLOCK ERASE command. The final bus WRITE operation latches the address of the block and starts the program/erase controller.

To erase multiple blocks (after the first two bus WRITE operations have selected the first block in the list), each additional block in the list can be selected by repeating the second bus WRITE operation using the address of the additional block. Any command except BLOCK ERASE or BLOCK SUSPEND during a timeout period resets that block to the read mode. The system can monitor DQ3 to determine if the block erase timer has timed out.

The UNLOCK BYPASS BLOCK ERASE command behaves the same way as the BLOCK ERASE command: the operation cannot be aborted, and a bus READ operation to the memory outputs the data polling register

ERASE SUSPEND command

The ERASE SUSPEND (B0h) command temporarily suspends a BLOCK ERASE operation. One bus WRITE operation is required to issue the command. The block address is “Don’t Care.”

The program/erase controller suspends the ERASE operation within the erase suspend latency time of the ERASE SUSPEND command being issued. However, when the ERASE SUSPEND command is written during the block erase timeout, the device immediately terminates the timeout period and suspends the ERASE operation. After the program/erase controller has stopped, the device operates in read mode, and the erase is suspended.
During an ERASE SUSPEND operation, it is possible to execute these operations in arrays that are not suspended:

- READ (main memory array)
- PROGRAM
- WRITE TO BUFFER PROGRAM
- AUTO SELECT
- READ CFI
- UNLOCK BYPASS
- Extended memory block commands
- READ/RESET

Reading from a suspended block will output the data polling register. If an attempt is made to program in a protected or suspended block, the PROGRAM command is ignored and the data remains unchanged; also, the data polling register is not read and no error condition is given.

Before the RESUME command is initiated, the READ/RESET command must be issued to exit AUTO SELECT and READ CFI operations. In addition, the EXIT UNLOCK BYPASS and EXIT EXTENDED MEMORY BLOCK commands must be issued to exit unlock bypass mode and the extended memory block mode.

An ERASE SUSPEND command is ignored if it is written during a CHIP ERASE operation.

If the ERASE SUSPEND operation is aborted by performing a device hardware reset or power-down, data integrity cannot be ensured, and it is recommended that the suspended blocks be erased again.

ERASE RESUME command

The ERASE RESUME (30h) command restarts program/erase controller after an ERASE SUSPEND operation.

The device must be in read mode before the RESUME command will be accepted.
An erase can be suspended and resumed more than once.

BLANK CHECK Operation

BLANK CHECK commands

Two commands are required to execute a BLANK CHECK operation: BLANK CHECK SETUP (EBh/76h) and BLANK CHECK CONFIRM AND READ (29h).

The BLANK CHECK operation determines whether a specific block is blank (that is, completely erased).
It can also be used to determine whether a previous ERASE operation was successful, including ERASE operations that might been interrupted by power loss.

The BLANK CHECK operation checks for cells that are programmed or over-erased. If it finds any, it returns a failure status, indicating that the block is not blank. If it returns a passing status, the block is guaranteed blank (all 1s) and is ready to program.

Before executing, the ERASE operation initiates an embedded BLANK CHECK operation, and if the target block is blank, the ERASE operation is skipped, benefitting overall cycle performance; otherwise, the ERASE operation continues.

The BLANK CHECK operation can occur in only one block at a time, and during its execution, reading the data polling register is the only other operation allowed. Reading from any address in the device enables reading the data polling register to monitor blank check progress or errors. Operations such as READ (array data), PROGRAM, ERASE, and any suspended operation are not allowed.

After the BLANK CHECK operation has completed, the device returns to read mode unless an error has occurred. When an error occurs, the device continues to output data polling register data. A READ/RESET command must be issued to reset the error condition and return the device to read mode.

Block Protection Command Definitions – Address-Data Cycles

Table 20. Block Protection Command Definitions – Address-Data cycles (x8, x16)

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		…	nth		
		A	D	A	D	A	D	A	D		A	D	
LOCK REGISTER Commands													
ENTER LOCK REGISTER COMMAND SET (40h)	X8	AAA	AA	555	55	AAA	40						3
	X16	555		2AA		555							
PROGRAM LOCK REGISTER (A0h)	X8	X	A0	X	Data								5
	X16												
READ LOCK REGISTER	X8	X	Data										4, 5, 6
	X16												
EXIT LOCK REGISTER (90h/00h)	X8	X	90	X	00								3
	X16												
PASSWORD PROTECTION Commands													
ENTER PASSWORD PROTECTION COMMAND SET (60h)	X8	AAA	AA	555	55	AAA	60						**3**
	X16	555	AA	2AA	55	555							
PROGRAM PASSWORD (A0h)	X8	X	A0	PWAn	PWDn								**7**
	X16												
READ PASSWORD	X8	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3	…	07	PWD 7	**4, 6, 8, 9**
	X16	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3				
UNLOCK PASSWORD (25h/03h)	X8	00	25	00	03	00	PWD 0	01	PWD 1	…	00	29	**8, 10**
	X16												
EXIT PASSWORD PROTECTION (90h/00h)	X8	X	90	X	00								**3**
	X16												

Block Protection Command Definitions – Address-Data cycles (x8, x16) (Continued)

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		…	nth		
		A	D	A	D	A	D	A	D		A	D	
NONVOLATILE PROTECTION Commands													
ENTER NONVOLATILE PROTECTION COMMAND SET (C0h)	X8	AAA	AA	555	55	AAA	C0						**3**
	X16	555		2AA		555							
PROGRAM NONVOLATILE PROTECTION BIT (A0h)	X8	X	A0	BAd	00								**11**
	X16												
READ NONVOLATILE PROTECTION BIT STATUS	X8	BAd	READ (DQ0)										**4, 6, 11**
	X16												
CLEAR ALL NONVOLATILE PROTECTION BITS (80h/30h)	X8	X	80	00	30								**12**
	X16												
EXIT NONVOLATILE PROTECTION BIT (90h/00h)	X8	X	90	X	00								**3**
	X16												
NONVOLATILE PROTECTION BIT LOCK BIT Commands													
ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h)	X8	AAA	AA	555	55	AAA	50						**3**
	X16	555		2AA		555							
PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h)	X8	X	A0	X	00								**11**
	X16												
READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS	X8	X	READ (DQ0)										**4, 6, 11**
	X16												
EXIT NONVOLATILE PROTECTION BIT LOCK BIT (90h/00h)	X8	X	90	X	00								**3**
	X16												

Block Protection Command Definitions – Address-Data cycles (x8, x16) (Continued)

Command and Code/Subcode	Bus Size	Address and Data Cycles											Notes
		1st		2nd		3rd		4th		…	nth		
		A	D	A	D	A	D	A	D		A	D	
VOLATILE PROTECTION Commands													
ENTER VOLATILE PROTECTION COMMAND SET (E0h)	X8	AAA	AA	555	55	AAA	E0						**3**
	X16	555		2AA		555							
PROGRAM VOLATILE PROTECTION BIT (A0h)	X8	X	A0	BAd	00								**11**
	X16												
READ VOLATILE PROTECTION BIT STATUS	X8	BAd	READ (DQ0)										**4, 6**
	X16												
CLEAR ALL NONVOLATILE PROTECTION BITS (A0h)	X8	X	A0	BAd	01								**11**
	X16												
EXIT NONVOLATILE PROTECTION BIT (90h/00h)	X8	X	90	X	00								**3**
	X16												
EXTENDED MEMORY BLOCK Operations													
ENTER EXTENDED MEMORY BLOCK (88h)	X8	AAA	AA	555	55	AAA	88						
	X16	555		2AA		555							
PROGRAM EXTENDED MEMORY BLOCK (A0h)	X8	AAA	AA	555	55	AAA	A0	Word address	data				
	X16	555		2AA		555							
READ EXTENDED MEMORY BLOCK	X8	Word address	data										
	X16												
EXIT EXTENDED MEMORY BLOCK (90h/00h)	X8	AAA	AA	555	55	555	90	X	00				
	X16	555		2AA									

Notes:

1. Key: A = Address and D = Data; X = “Don’t Care; BAd = Any address in the block; PWDn = Password bytes, n = 0 to 7 (x8)/ words 0 to 3 (x16); PWAn = Password address, n = 0 to 3(x16); Gray = Not applicable. All values in the table are hexadecimal.
2. DQ[15:8] are “Don’t Care” during UNLOCK and COMMAND cycles. A[MAX:16] are “Don’t Care” during UNLOCK and COMMAND cycles, unless an address is required

3. The ENTER command sequence must be issued prior to any operation. It disables READ and WRITE operations from and to all blocks in the main array. Also, when an ENTER COMMAND SET command is issued, an EXIT COMMAND SET command must be issued to return the device to READ mode.
4. READ REGISTER/PASSWORD commands have no command code; CE# and OE# are driven LOW and data is read according to a specified address.
5. Data = Lock Register content
6. All address cycles shown for this command are READ cycles
7. Only one portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.
8. Each portion of the password can be entered or read in any order as long as the entire 64-bit password is entered or read.
9. For the x8 READ PASSWORD command, the nth (and final) address cycle equals the 8^{th} address cycle. From the 5^{th} to the 8^{th} address cycle, the values for each address and data pair continue the pattern shown in the table as follows: for x8, address and data = 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.
10. For the x8 UNLOCK PASSWORD command, the nth (and final) address cycle equals the 11^{th} address cycle. From the 5^{th} to the 10^{th} address cycle, the values for each address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3; 04 and PWD4; 05 and PWD5; 06 and PWD6; 07 and PWD7.

    For x16 UNLOCK PASSWORD command, the nth (and final) address cycle equals the 7^{th} address cycle. For the 5^{th} and 6^{th} address cycles, the values for the address and data pair continue the pattern shown in the table as follows: address and data = 02 and PWD2; 03 and PWD3.
11. Both nonvolatile and volatile protection bit settings are as follows: Protected state = 00; Unprotected state = 01.
12. The CLEAR ALL NONVOLATILE PROTECTION BITS command programs all nonvolatile protection bits before ensure. This prevents over-erasure of previously cleared nonvolatile protection bits.

PROTECTION OPERATIONS

Blocks can be protected individually against accidential PROGRAM, ERASE, or READ operations on both 8-bit and 16-bit configurations. The block protection scheme is shown in the Software Protection Scheme figure.

Memory block and extended memory block protection is configured through the lock register.

Lock Register Commands

After the ENTER LOCK REGISTER COMMAND SET (40h) command has been issued, all bus READ or PROGRAM operations can be issued to lock register.

The PROGRAM LOCK REGISTER (A0h) command allows the lock register to be configured. The programmed data can then be checked with a READ LOCK REGISTER command by driving CE# and OE# LOW with the appropriate address data on the address bus.

Password Protection Commands

After the ENTER PROTECTION COMMAND SET (60h) command has been issued, the commands related to password protection mode can be issued to the device.

The PROGRAM PASSWORD (A0h) command is used to program the 64-bit password used in the password protection mode. To program the 64-bit password, the complete command sequence must be entered eight times at eight consecutive address selected by A[1:0] plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A[1:0] in 16-bit mode. By default, all password bits are set to 1. The password can be checked by issuing a READ PASSWORD command.

The READ PASSWORD command is used to verify the password used in password protection mode. To verify the 64-bit password, the complete command sequence must be entered eight times at eight consecutive address selected by A[1:0] plus DQ15/A-1 in 8-bit mode, or four times at four consecutive addresses selected by A[1:0] in 16-bit mode. If the password mode lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

The UNLOCK PASSWORD (25/03h) command is used to clear the nonvolatile protection bit lock bit, allowing the nonvolatile protection bits to be modified. The UNLOCK
PASSWORD command must be issued, along with the correct password, and requires a **1us** delay between successive UNLOCK PASSWORD commands in order to prevent hackers from cracking the password by trying all possible 64-bit combinations. If this delay does not occur, the last command will be ignored. Approximately **1us** is required for unlocking the device after the valid 64bit password has been provided.

Nonvolatile Protection Commands

After the ENTER NONVOLATILE PROTECTION COMMAND SET (C0h) command has been issued, the commands related to nonvolatile protection mode can be issued to the device.

A block can be protected from program or erase by issuing a PROGRAM NONVOLATILE PROTECTION BIT (A9h) command, along with the block address. This command sets the nonvolatile protection bit to 0 for a given block. The status of a nonvolatile protection bit for a given block or group of blocks can be read by issuing a READ NONVOLATILE MODIFY PROTECTION BIT command, along with the block address.

The nonvolatile protection bits are erased simultaneously by issuing a CLEAR ALL NONVOLATILE PROTECTION BITS (80/30h) command. No specific block address is required. If the nonvolatile protection bit block bit is set to 0, the command fails.

Nonvolatile Protection Bit Lock Bit Commands

After the ENTER NONVOLATILE PROTECTION BIT LOCK BIT COMMAND SET (50h) command has been issued, the commands that allow the nonvolatile protection bit lock bit to be set can be issued to the device.

The PROGRAM NONVOLATILE PROTECTION BIT LOCK BIT (A0h) command is used to set the nonvolatile protection bit lock bit to 0, thus locking the nonvolatile protection bits and preventing them from being modified.

The READ NONVOLATILE PROTECTION BIT LOCK BIT STATUS command is used to read the status of the nonvolatile protection bit lock bit.

Volatile Protection Commands

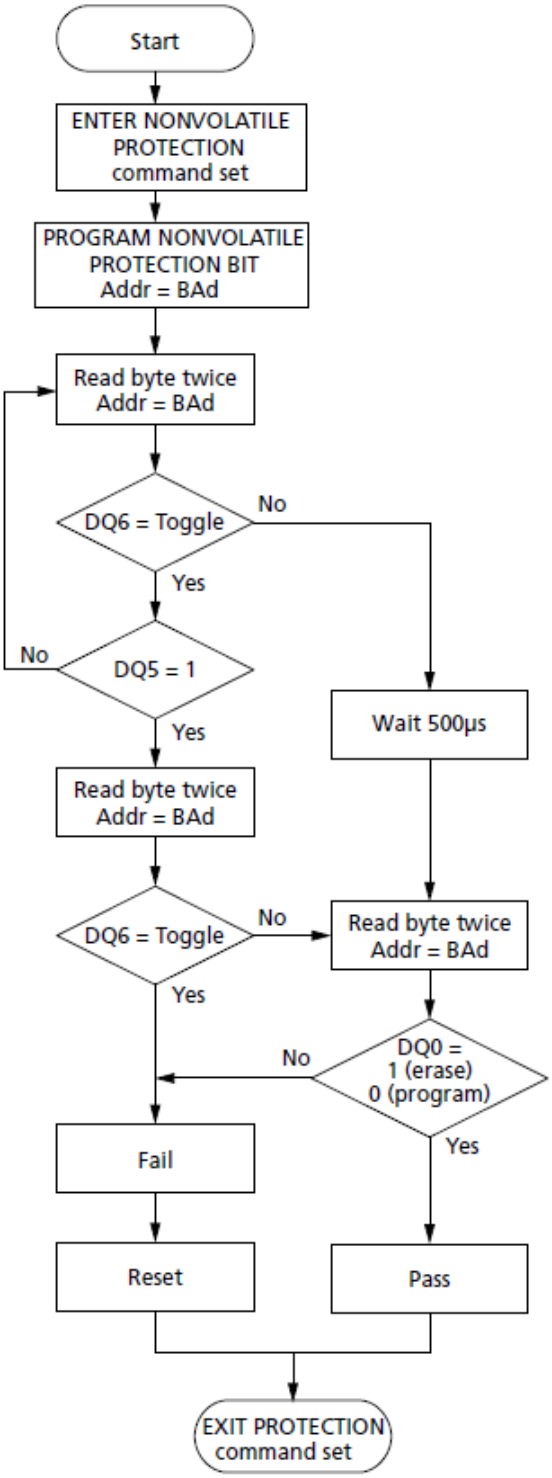
After the ENTER VOLATILE PROTECTION BIT LOCK BIT COMMAND SET (E0h) command has been issued, the commands that allow the volatile protection mode can be issued to the device.

The PROGRAM VOLATILE PROTECTION BIT (A0h) command individually sets a volatile protection bit to 0 for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit.

The status of a volatile protection bit for a given block can be read by issuing a READ VOLATILE PROTECTION BIT STATUS command along with the block address.

The CLEAR VOLATILE PROTECTION BIT (A0h) command individually clears (sets to 1) the volatile protection bit for a given block. If the nonvolatile protection bit for the same block is set, the block is locked regardless of the value of the volatile protection bit.

Figure 13. Program/Erase Nonvolatile Protection Bit Algorithm



Extended Memory Block Commands

The device has one extra 128-word extended memory block that can be accessed only by the ENTER EXTENDED MEMORY BLOCK (88h) command. The extended memory block is 128 words (x16) or 256 bytes (x8). It is used as a security block to provide a permanent 128-bit security identification number or to store additional information. The device can be shipped with the extended memory block prelocked permanently by ISSI, including 128-bit security identification number. Or, the device can be shipped with the extended memory block unlocked, enabling customers to permanently program and lock it.

After the ENTER EXTENDED MEMORY BLOCK command has been issued, the device enters the extended memory block mode. All bus READ or PROGRAM operations are conducted on the extended memory block, and the extended memory block is addressed using the address occupied by the block 0 in other operating modes.

In extended memory block mode, ERASE, CHIP ERASE, CHIP ERASE SUSPEND, and ERASE RESUME commands are not allowed. The extended memory block cannot be erased, and each bit of the extended memory block can only be programmed once.

The extended memory block is protected from further modification by programming lock register bit 0. Once invoked, this protection cannot be undone.

The device remains in extended memory block mode until the EXTENDED MEMORY BLOCK (90/00h) command is issued, which returns the device to read mode, or until power is removed from the device. After a power-up sequence or hardware reset, the device will revert to reading memory blocks in the main array.

Table 23. Extended Memory Block Address and Data

Address			Data	
X8	**X16**	**ISSI prelocked**	**Customer Lockable**	
000000h-00000Fh	000000h-000007h	Secure ID number	Determined by customer	Secure ID number
000010h-0000FFh	000008h-00007Fh	Protected and unavailable		Determined by customer

Exit Protection Command

The EXIT PROTECTION COMMAND SET (90/00h) command is used to exit the lock register, password protection, nonvolatile protection, and nonvolatile protection bit lock bit command set modes and return the device to read mode.

DEVICE PROTECTION

Hardware Protection

The Vpp/WP# function provides a hardware method of protecting either the highest/lowest block or the top/bottom two blocks. When Vpp/WP# is LOW, PROGRAM/ERASE operations on either of these block options is ignored to provide protection.
When Vpp/WP# is HIGH, the device reverts to the previous protection status for the highest/lowest block or top/bottom two blocks. PROGRAM and ERASE operations can modify the data in either of these block options unless block protection is enabled.

Note: It is highly recommended that driving Vpp/WP# HIGH or LOW. Vpp/WP# has a resistive pullup controlled by a latch, which is reset to the VIH state during Vcc power up; when unconnected, Vpp/WP# will remain at VIH.

Table 24. Vpp/WP# Functions

Vpp/WP# Settings	Function
V_{IL}	Highest/Lowest block or the Top/Bottom two blocks are protected.
V_{IH}	Highest/Lowest block or the Top/Bottom two blocks are unprotected unless software protection is activated.

Software Protection

The following software protection modes are available:

- Volatile protection
- Nonvolatile protection
- Password protection
- Password access

The device is shipped from the factory with all blocks unprotected. On first use, the device defaults to the nonvolatile protection mode but can be activated in either the nonvolatile protection or password protection mode.

The desired protection mode is activated by setting either the nonvolatile protection mode lock bit or the password protection mode lock bit of the lock register. Both bits are one-time-programmable and nonvolatile; therefore, after the production mode has been activated, it cannot be changed, and the device is set permanently to operate in the selected production mode. It is recommended that the desired software protection mode be activated when first programming the device.

For the lowest and highest blocks or for top/bottom two blocks, a higher level of block protection can be achieved by locking the blocks using nonvolatile protection mode and holding Vpp/WP# LOW.

Blocks with volatile protection and nonvolatile protection can coexist within the memory array. If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The block protection status can be read by performing a read electronic signature or by issuing an AUTO SELECT command.

Volatile Protection Mode

Volatile protection enables the software application to protect blocks against inadvertent change and can be disabled when changes are needed. Volatile protection bits are unique for each block and can be individually modified. Volatile protection bits control the protection scheme only for unprotected blocks whose nonvolatile protection bits are cleared to 1. Issuing a PROGRAM VOLATILE PROTECTION BIT or CLEAR VOLATILE PROTECTION BIT command sets to 0 or clears to 1 the volatile protection bits and places the associated blocks in the protected (0) or unprotected (1) state, respectively. The volatile protection bit can be set or cleared as often as needed.

When the device is first shipped, or after a power-up or hardware reset, the volatile protection bits default to 1 (unprotected).

Nonvolatile Protection Mode

A nonvolatile protection bit is assigned to each block. Each of these bits can be set for protection individually by issuing a PROGRAM NONVOLATILE PROTECTION BIT command. Also, each device has one global volatile bit called the nonvolatile protection bit lock bit; it can be set to protect all nonvolatile protection bits at once. This global bit must be set to 0 only after all nonvolatile protection bits are configured to the desired settings. When set to 0, the nonvolatile protection bit lock bit prevents changes to the state of the nonvolatile protection bits. When cleared to 1, the nonvolatile protections can be set and cleared using the PROGRAM NONVOLATILE PROTECTION BIT and CLEAR ALL NONVOLATILE PROTECTION BITS commands, respectively.

No software command unlocks the nonvolatile protection bit lock bit unless the device is in password protection mode; in nonvolatile protection mode, the nonvolatile protection bit lock bit can be cleared only by taking the device through a hardware reset or power-up.

If one of the nonvolatile protection bits needs to be cleared (unprotected), additional steps are required: First, the nonvolatile protection bit lock bit must be cleared to 1, using either a power-cycle or hardware reset. Then, the nonvolatile protection bits can be changed to reflect the desired settings. Finally, the nonvolatile protection bit lock bit must be set to 0 to lock the nonvolatile protection bits. The device now will operate normally.

To achieve the best protection, the PROGRAM NONVOLATILE PROTECTION LOCK BIT command should be executed early in the boot code, and the boot code should be protected by holding Vpp/WP# LOW.

Nonvolatile protection bits and volatile protection bits have the same function when Vpp/WP# is HIGH or when Vpp/WP# is HIGH or when Vpp/WP# is at the voltage for program acceleration (V_{PPH}).

Password Protection Mode

The password protection mode provides a higher level of security than the nonvolatile protection mode by requiring a 64-bit password to unlock the nonvolatile protection lock bit. In addition to this password requirement, the nonvolatile protection bit lock bit is set to 0 after power-up and reset to maintain the device in password protection mode.

Executing the UNLOCK PASSWORD command by entering the correct password clears the nonvolatile protection bit lock bit, enabling the block nonvolatile protection bits to be modified. If the password provided is incorrect, the nonvolatile protection bit lock bit remains locked, and the state of the nonvolatile protection bits cannot be modified.

To place the device in password protection mode, the following two steps are required:

- First, before activating the password protection mode, a 64-bit password must be set and the setting verified. Password verification is allowed only before the password protection mode is activated.
- Next, password protection mode is activated by programming the password protection mode lock bit to 0. This operation is irreversible.

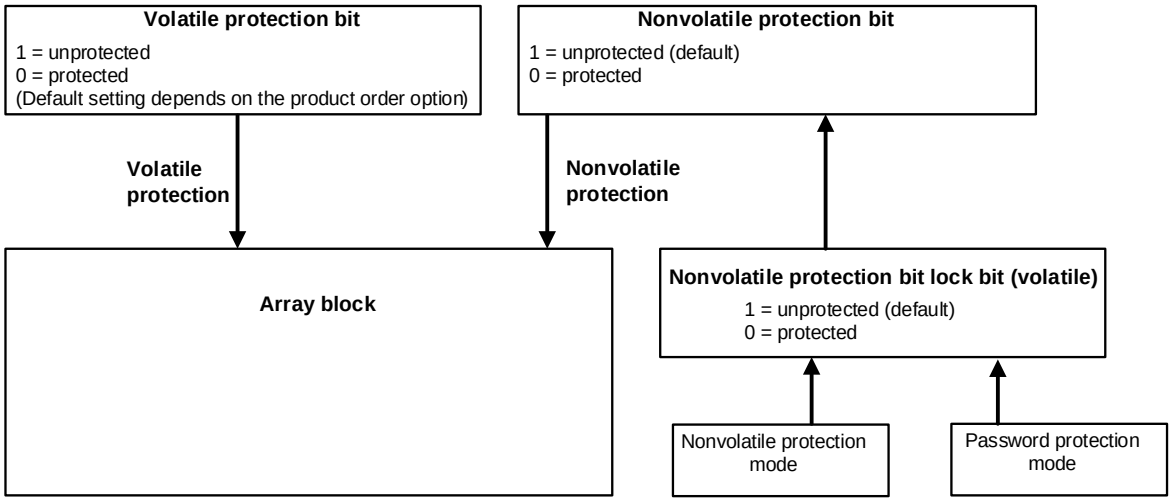
After the bit is programmed, it cannot be erased, the device remains permanently in password protection mode, and the 64-bit password can be neither retrieved nor reprogrammed. In addition, all commands to the address where the password is stored are disabled.

Note: There is no means to verify the password after password protection mode is enabled. If the password is lost after enabling the password protection mode, there is no way to clear the nonvolatile protection bit lock bit.

Password Access

Password access is a security enhancement that protects information stored in the main array blocks by preventing content alteration or reads until a valid 64-bit password is received. Password access may be combined with nonvolatile and/or volatile protection to create

Figure 14. Software Protection Scheme



Note: Volatile protection bits are programmed and cleared individually. Nonvolatile protection bits are programmed individually and cleared collectively.

COMMON FLASH INTERFACE (CFI)

The common flash interface (CFI) specification outlines device and host systems software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the READ CFI QUERY command is issued, and the data structure is read from memory. The following tables show the address (A-1, A [7:0]) used to retrieve the data. The query data is always presented on the lowest order data outputs (DQ [7:0]), and the other data outputs (DQ [15:8]) are set to 0.

Table 25. Query Structure Overview

Addresses		Subsection Name	Description
X16	X8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System Interface information	Device timing and voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algothrithm-specific extended query table	Additional information specific to the primary algorithm (optional)

Note: Query data are always presented on the lowest order data outputs (DQ [7:0]). DQ [15:8] are set to 0.

Table 26. CFI Query Identification String

Addresses		Data	Description
X16	X8		
10h	20h	0051h	Query Unique ASCII string “QRY”
11h	22h	0052h	
12h	24h	0059h	
13h 14h	26h 28h	0002h 0000h	Primary algorithm command set and control interface ID code 16-bit ID code defining a specific algorithm
15h 16h	2Ah 2Ch	0040h 0000h	Address for primary algorithm extended query table
17h 18h	2Eh 30h	0000h 0000h	Alternate vendor command set and control interface ID code second vendor-specified algorithm supported
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate algorithm extended query table

Note: Query data are always presented on the lowest order data outputs (DQ [7:0]). DQ [15:8] are set to 0.

Table 27. System Interface String

Addresses		Data	Description	Value
X16	X8			
1Bh	36h	0027h	Vcc Min (write/erase) DQ7-DQ4: volt, DQ3-DQ0: 100mV	2.7V
1Ch	38h	0036h	Vcc Max (write/erase) DQ7-DQ4: volt, DQ3-DQ0: 100mV	3.6V
1Dh	3Ah	0095h	V_{PPH} Min voltage (00h = no Vpp pin present)	9.5V
1Eh	3Ch	00A5h	V_{PPH} Max voltage (00h = no Vpp pin present)	10.5V
1Fh	3Eh	0004h	Typical timeout per single byte/word write 2^N µs	16us
20h	40h	000Ah	Typical timeout for min size buffer write 2^N µs (00h = not supported)	1024us
21h	42h	0009h	Typical timeout per individual block erase 2^N ms	0.5s
22h	44h	000Eh	Typical timeout for full chip erase 2^N ms (00h = not supported)	16Mb:17s
		000Fh		32Mb:33s
		0010h		64Mb:66s
23h	46h	0004h	Max timeout for byte/word write 2^N times typical	256us
24h	48h	0002h	Max timeout for buffer write 2^N times typical	4096us
25h	4Ah	0003h	Max timeout per individual block erase 2^N times typical	4s
26h	4Ch	0002h	Max timeout for full chip erase 2^N times typical (00h = not supported)	16Mb:66s
		0002h		32Mb:131s
		0002h		64Mb:262s

Table 28. Device Geometry Definition

Addresses		Data	Description	Value
X16	X8			
27h	4Ehh	0015h	Device Size = 2^N bytes, 0016h for 32Mb	2MB
		0016h		4MB
		0017h		8MB
28h 29h	50h 52h	0002h 0000h	Flash Device Interface Description 01h = X16 only; 02h = x8/x16	X8, x16 asynchronous
2Ah 2Bh	54h 56h	0008h(1) 0000h	Max number of bytes in multi-byte program or page = 2^N (00h = not supported)	256
2Ch	58h	See table below	Number of Erase Block Regions. It specifies the number of regions containing contiguous blocks of the same size. 01h = Uniform device, 02h = Boot device	-
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	See table below	Erase Block Region 1 Information Bits[15:0] = y, y+1 = Number of identical-size erase blocks Bits[31:16] = z, block size in region 1 is z x 256 bytes	-
31h 32h 33h 34h	62h 64h 66h 68h	See table below	Erase Block Region 2 Information Bits[15:0] = y, y+1 = Number of identical-size erase blocks Bits[31:16] = z, block size in region 1 is z x 256 bytes	-
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information	-
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information	-

Note: The value at 2Ah in the CFI region is set to 08h (256 bytes) due to compatibility issues. The maximum 256-word program buffer can be used to optimize system program performance.

Table 29. Erase Block Region Information

Address	16Mb			32Mb			64Mb		
	Top	Bottom	Uniform	Top	Bottom	Uniform	Top	Bottom	Uniform
2Ch	02h	02h	01h	02h	02h	01h	02h	02h	01h
2Dh	07h	07h	1Fh	07h	07h	3Fh	07h	07h	7Fh
2Eh	00h	00h	00h	00h	00h	00h	00h	00h	00h
2Fh	20h	20h	00h	20h	20h	00h	20h	20h	00h
30h	00h	00h	01h	00h	00h	01h	00h	00h	01h
31h	1Eh	1Eh	00h	3Eh	3Eh	00h	7Eh	7Eh	00h
32h	00h	00h	00h	00h	00h	00h	00h	00h	00h
33h	00h	00h	00h	00h	00h	00h	00h	00h	00h
34h	01h	01h	00h	01h	01h	00h	01h	01h	00h

Table 30. Primary Algorithm-specific Extended Query

Addresses		Data	Description	Value
X16	X8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string "PRI"	"P"
41h	82h	0052h		"R"
42h	84h	0049h		"I"
43h	86h	0031h	Major version number, ASCII	"1"
44h	88h	0033h	Minor version number, ASCII	"3"
45h	8Ah	0100h	Address Sensitive Unlock (bits [1:0]) 00 = Required, 01 = Not Required Silicon revision number (bits [5:2]) 0001 = 0.18um, 0010 = 0.13um, 0011 = 90nm, 0100 = 65nm	Required
46h	8Ch	0002h	Erase Suspend: 00 = Not Supported, 01 = To Read Only, 02 = To Read & Write	2
47h	8Eh	0001h	Block Protection: 00 = Not Supported, X = Minimum number of blocks per group	1
48h	90h	0000h	Temporary block unprotect: 00 = Not Supported, 01 = Suported	Not supported
49h	92h	0008h	Block Protect/Unprotect: 08 = Advanced sector Protection	8
4Ah	94h	0000h	Simultaneous operations: 00 = Not Supported	Not supported
4Bh	96h	0000h	Burst mode: 00 = Not Supported	Not supported
4Ch	98h	0002h	Page Mode : 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page 03 = 16 Word Page	8 Word Page
4Dh	9Ah	0095h	V_{PPH} supply minimum program/erase voltage: Bits [7:4] hex value in volts, Bits [3:0] BCD value in 100mV.	9.5V
4Eh	9Ch	00A5h	V_{PPH} supply maximum program/erase voltage: Bits [7:4] hex value in volts, Bits [3:0] BCD value in 100mV.	10.5V
4Fh	9Eh	00xxh	Top/Bottom boot block flag: xx = 02h: Bottom boot device, HW protection for bottom two blocks xx = 03h: Top boot device, HW protection for top two blocks xx = 04h: Uniform device, HW protection for lowest block xx = 05h: Uniform device, HW protection for highest block	Device type (bottom boot, top boot, uniform)
50h	A0h	0001h	Program suspend: 00 = Not supported 01 = supported	Supported

POWER-UP and Reset Characteristics

Table 31: Power-Up Specifications

Parameter	Symbol		Min	Unit	Notes
	Legacy	JEDEC			
V_{CC} HIGH to V_{CCQ} HIGH	-	tVCHVCQH	0	us	1
V_{CC} HIGH to rising edge of RST#	tVCS	tVCHPH	60	us	2
V_{CCQ} HIGH to rising edge of RST#	tVIOS	tVCQHPH	0	us	2
RST# HIGH to chip enable LOW	tRH	tPHEL	50	ns	
RST# HIGH to write enable LOW	-	tPHWL	150	ns	

Notes:
1. VCC and VCCQ ramps must be synchronized during power-up.
2. If RST# is not stable for tVCS or tVIOS, the device will not allow any READ or WRITE operations, and a hardware reset is required.

Figure 15: Power-Up Timing

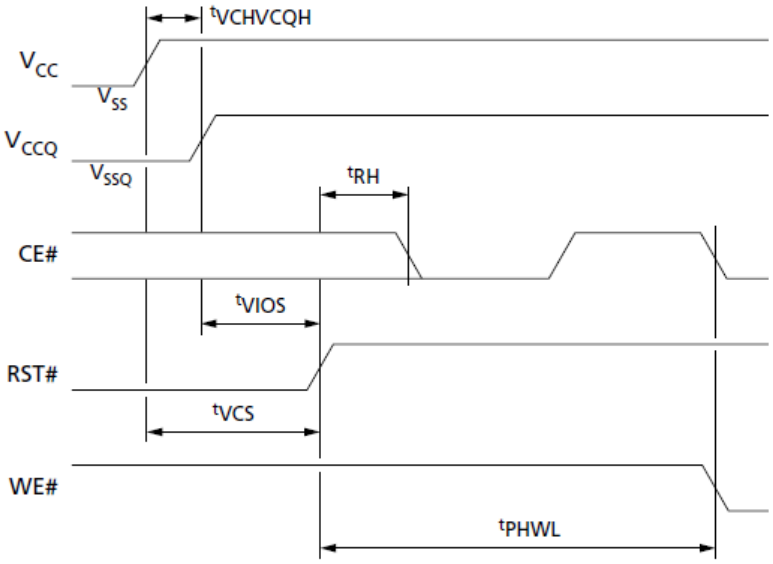


Table 32: Reset AC Specifications

Condition/Parameter	Symbol		Min	Max	Unit	Notes
	Legacy	JEDEC				
RST# LOW to read mode during program or erase	tREADY	tPLRH	-	25	us	1
RST# pulse width	tRP	tPLPH	100	-	ns	
RST# HIGH to CE# LOW, OE# LOW	tRH	tPHEL, tPHGL	50	-	ns	1
RST# LOW to standby mode during read mode	tRPD	-	10	-	us	
RST# LOW to standby mode during program or erase mode			50	-	us	
RY/BY# HIGH to CE# LOW, OE# LOW	tRB	tRHEL, tRHGL	0		ns	1

Notes:
1. Sampled only; not 100% tested.

Figure 16: Reset AC Timing – No PROGRAM/ERASE operation in Progress

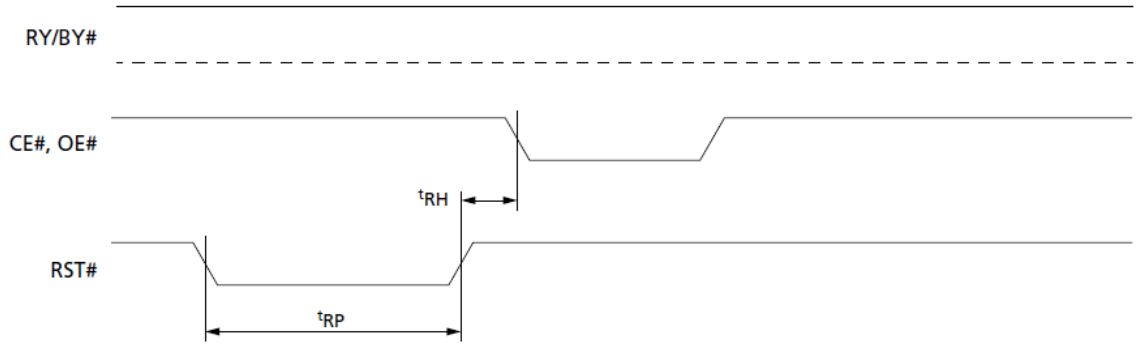
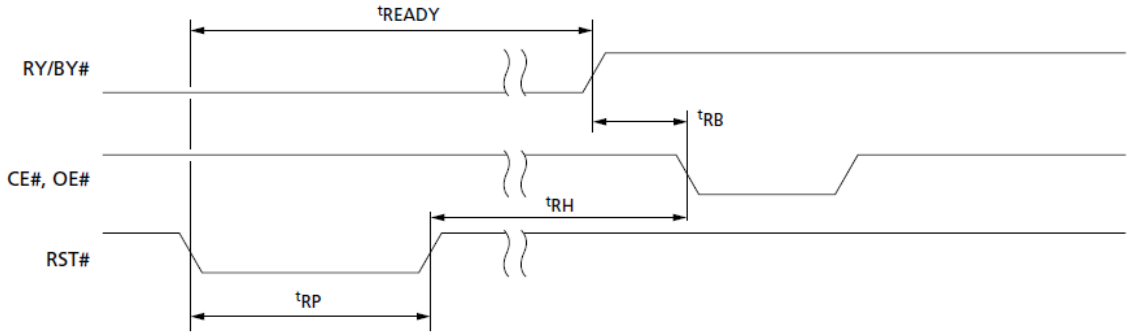


Figure 17: Reset AC Timing during PROGRAM/ERASE operation



ABSOLUTE MAXIMUM RATINGS

Parameter			Value	Notes
Storage Temperature			-65°C to +150°C	
Surface Mount Lead Soldering Temperature		Standard Package	240°C 3 Seconds	
		Lead-free Package	260°C 3 Seconds	
Voltage with Respect to Ground	Vcc, V_{CCQ}		-0.5V to 4.0V	
	Input/output voltage		-0.5V to V_{CCQ} + 0.5V	1, 2
	VPPH		-0.5V to 10.5V	1, 2

Notes:

1. During signal transition, minimum voltage may undershoot to -2V during periods less than 20ns.
2. During signal transition, maximum voltage may overshoot to V_{CC} + 2V during periods less than 20ns.

Table 33: OPERATING CONDITIONS

Parameter		Value
Ambient Operating Temperature (T_A)	Extended Grade	-40°C to 105°C
	Automotive Grade A3	-40°C to 125°C
V_{CC} Power Supply		2.7V (V_{CC}min) – 3.6V (V_{CC}max); 3.3V (Typ)
V_{CCQ} Power Supply		1.65V (V_{CCQ} min) – Vcc (V_{CCQ} max); 3.3V (Typ)
Load capacitance		30 pF
Input rise and fall times		2.5ns (max.)
Input pulse voltage		0 to V_{CCQ}
Input and output timing reference voltages		V_{CCQ}/2

Figure 18. Test Conditions

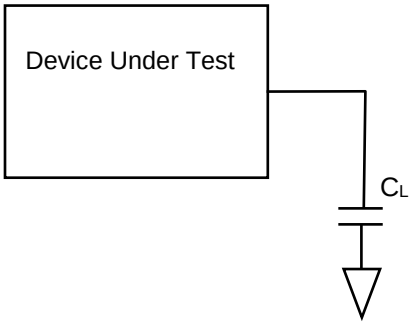


Figure 19. AC Measurement I/O Waveforms

Table 34: Input/Output Capacitance

Parameter	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	2	7	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	2	5	pF

Table 35. DC Characteristics

(Under recommended operating ranges)

Symbol	Parameter		Test Conditions		Min	Typ[4]	Max	Unit
I_{LI}[1]	Input Leakage Current		$0V \le V_{IN} \le Vcc$				±1	µA
I_{LO}	Output Leakage Current		$0V \le V_{OUT} \le Vcc$				±1	µA
I_{CC1}	V_{CC} Active Read Current	Random	CE# = V_{IL}; OE# = V_{IH}, V_{CC} = V_{CC}max, f=5MHz			20	25	mA
		Page	CE# = V_{IL}; OE# = V_{IH}, V_{CC} = V_{CC}max, f=13MHz			12	16	mA
I_{CC2}	V_{CC} Standby Current	64Mb	CE#, RST# = VCCQ ± 0.2 V, V_{CC} = V_{CC} max			35	120	µA
		32Mb				35	120	
		16Mb				35	100	
I_{CC3}[2]	V_{CC} Program/ Erase/Blank Check Current		program/erase controller active	Vpp/WP# = V_{IL} or V_{IH}		35	50	mA
				Vpp/WP# = V_{PPH}		26	33	
I_{PP1}	Read		Vpp/WP# ≤ V_{CC}		-	2	15	µA
	Standby				-	0.2	5	µA
I_{PP2}	Reset		RST# = V_{SS} ± 0.2 V			0.2	5	µA
I_{PP3}	Program operation ongoing		Vpp/WP# = 10V ± 5%		-	5	10	mA
			Vpp/WP# = V_{CC}		-	0.05	0.10	mA
I_{PP4}	Erase operation ongoing		Vpp/WP# = 10V ± 5%		-	5	10	mA
			Vpp/WP# = V_{CC}		-	0.05	0.10	mA
V_{IL}	Input Low Voltage		-		-0.1		0.3 x V_{CCQ}	V
V_{IH}	Input High Voltage		-		0.7 x V_{CCQ}		V_{CCQ} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 100µA		-	-	0.15 x V_{CCQ}	V
V_{OH}	Output High Voltage CMOS		I_{OH} = -100µA		0.85 x V_{CCQ}		-	V
V_{PPH}	Acceleration Program Voltage		-		9.5		10.5	V
V_{PPL}	V_{PP} logic level		-		2.7		3.6	
V_{LKO}[2]	Program/erase lockout supply voltage		-		2.3	-	-	V

Notes:

1. The maximum input leakage current is ± 5 uA on the Vpp/WP# pin.
2. Sampled only; not 100% tested.

AC CHARACTERISTICS

Table 36. Read-only Operations Characteristics

Parameter Symbols		Description	Condition	Package	Min	Max	Unit
JEDEC	Legacy						
t_{AVAV}	t_{RC}	Read Cycle Time	$V_{CCQ} \geq 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	60	-	ns
				TSOP	70	-	
			$V_{CCQ} \leq 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	65	-	ns
				TSOP	75	-	
t_{AVQV}	t_{ACC}	Address valid to output valid	$V_{CCQ} \geq 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	-	60	ns
				TSOP	-	70	
			$V_{CCQ} \leq 2.7V$, CE# = V_{IL}, OE# = V_{IL}	BGA	-	65	ns
				TSOP	-	75	
t_{AVQV1}	t_{PAGE}	Address to output valid (page)	CE# = V_{IL}, OE# = V_{IL}	BGA	-	25	ns
				TSOP	-	25	
t_{ELQX}(1)	t_{LZ}(1)	CE# LOW to output transition	OE# = V_{IL}	BGA	0	-	ns
				TSOP	0	-	
t_{ELQV}	t_{E}	CE# LOW to output valid	$V_{CCQ} \geq 2.7V$, OE# = V_{IL}	BGA	-	60	ns
				TSOP	-	70	
			$V_{CCQ} \leq 2.7V$, OE# = V_{IL}	BGA	-	65	ns
				TSOP	-	75	
T_{OLZ}(1)	T_{OLZ}(1)	OE# LOW to output transition	CE# = V_{IL}	BGA	0	-	ns
				TSOP	0	-	
T_{GLQV}	T_{OE}	OE# LOW to output valid	CE# = V_{IL}	BGA	-	25	ns
				TSOP	-	25	
t_{EHQZ}(1)	T_{HZ}(1)	CE# HIGH to output transition	OE# = V_{IL}	BGA	-	20	ns
				TSOP	-	20	
T_{GHQZ}(1)	T_{DF}(1)	CE# HIGH to output transition	CE# = V_{IL}	BGA	-	15	ns
				TSOP	-	15	
t_{EHQX}, t_{EHQX}, t_{EHQX}	T_{OH}	CE#, OE#, or address transition to output transition.	-	BGA	0	-	ns
				TSOP	0	-	
T_{ELBL}	T_{ELFL}	CE# to BYTE# LOW.	-	BGA	-	10	ns
				TSOP	-	10	
T_{ELBH}	T_{ELFH}	CE# to BYTE# HIGH.	-	BGA	-	10	ns
				TSOP	-	10	
T_{BLQV}	T_{FLQV}	BYTE# LOW to output valid	-	BGA	-	1	us
				TSOP	-	1	
T_{BHQV}	T_{FHQV}	BYTE# HIGH to output valid.	-	BGA	-	1	us
				TSOP	-	1	
T_{BLQZ}	T_{FLQZ}	BYTE# LOW to output in High-Z	-	BGA	-	1	us
				TSOP	-	1	

Note:
1. Sampled only; not 100% tested.

Figure 20. Random Read AC Timing (x8 Mode)

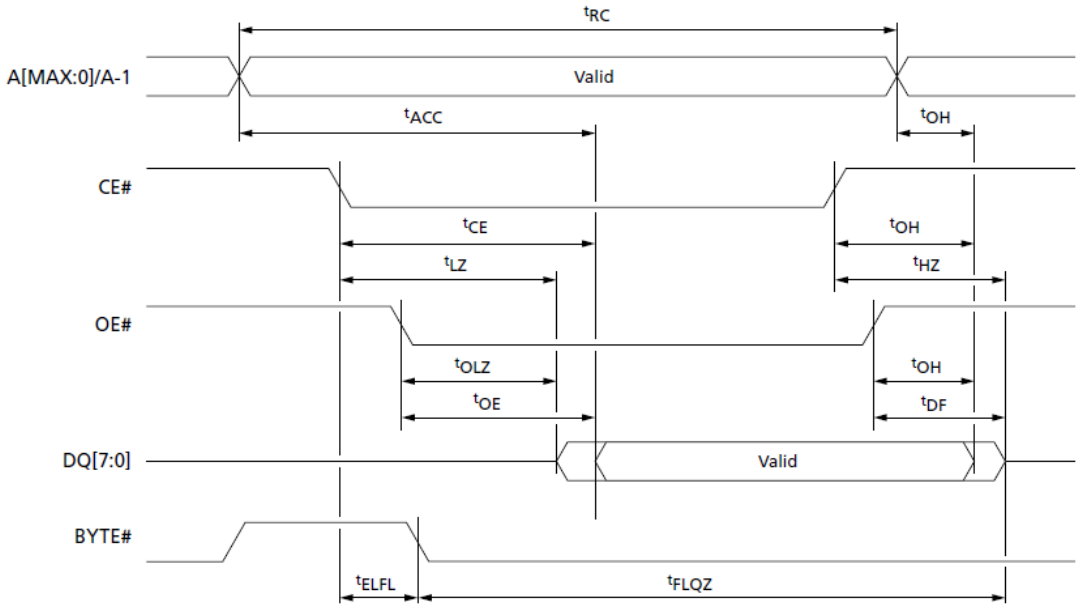


Figure 21. Random Read AC Timing (x16 Mode)

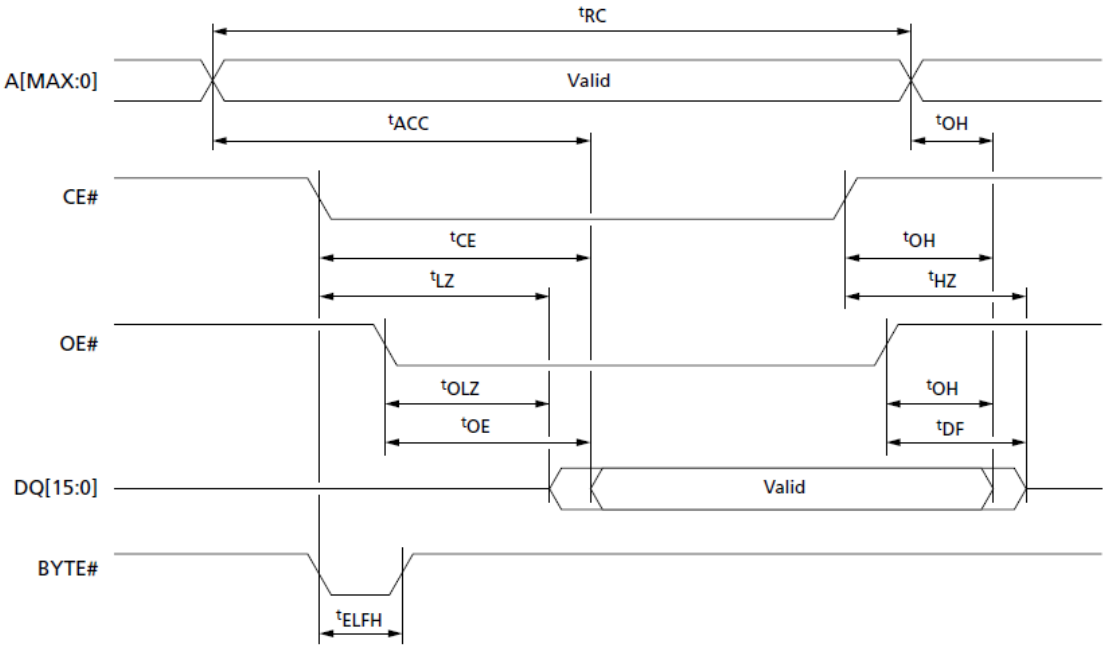


Figure 22. BYTE# Transition Read AC Timing

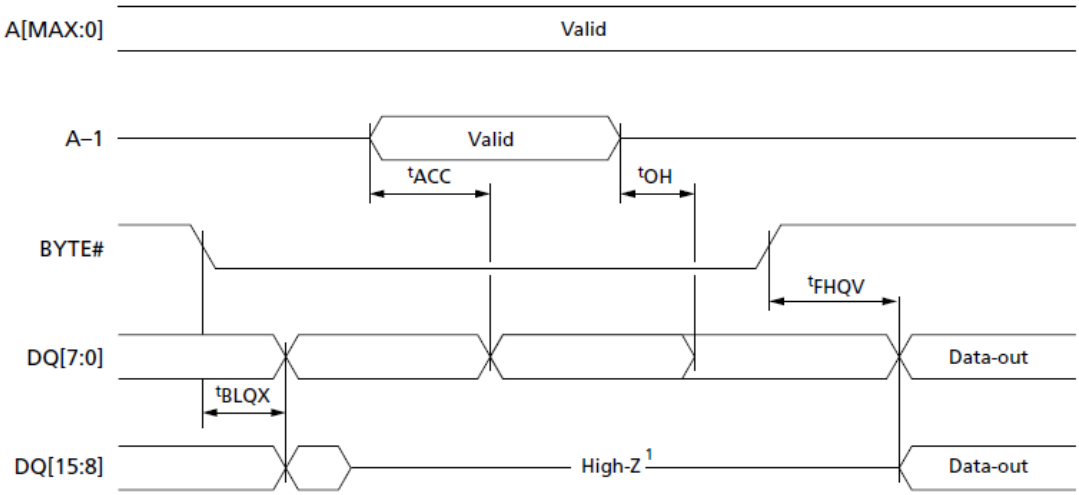
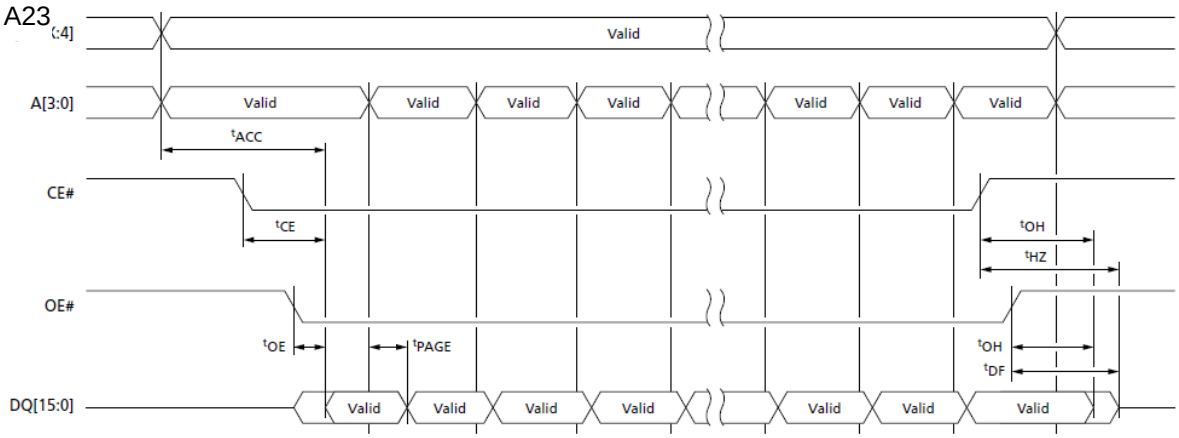


Figure 23. Page Read Operation Timings



Note: Page size is 8 words (16 bytes) and is addressed by address inputs A [2:0] in x16 bus mode and A[2:0] + DQ 15/A-1 in x8 mode.

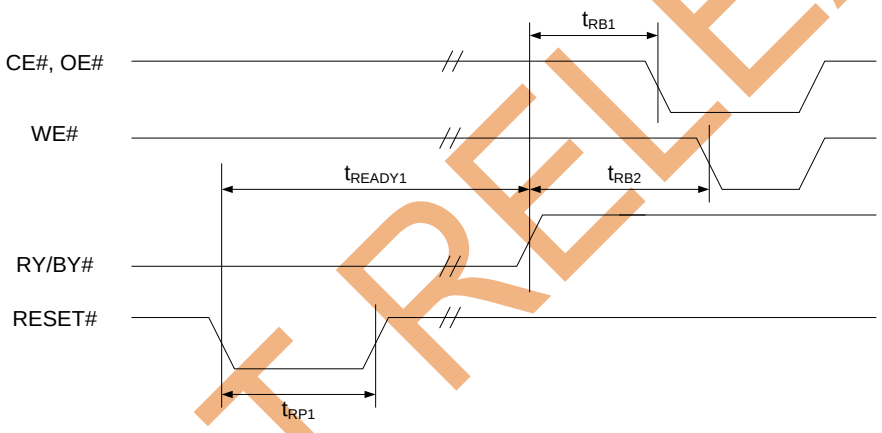
AC CHARACTERISTICS

Table 37. Hardware Reset (RESET#)

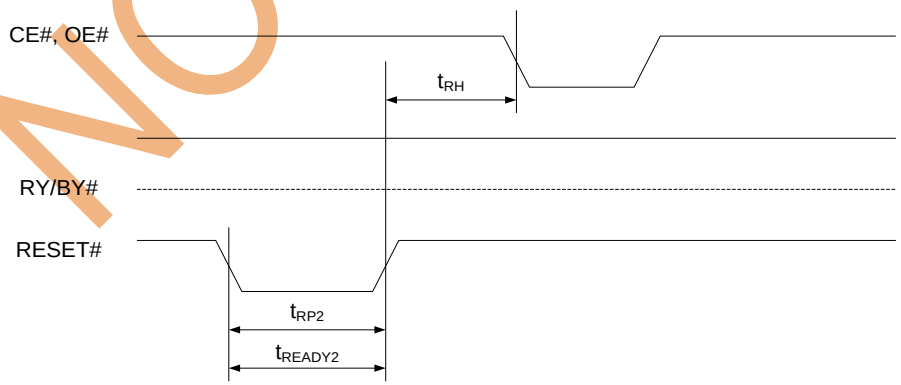
(Under recommended operating ranges)

Parameter Std	Description	Test Setup	Speed	Unit
			60/70ns	
t_{RP1}	RESET# Pulse Width (During Embedded Algorithms)	Min	200	ns
t_{RP2}	RESET# Pulse Width (NOT During Embedded Algorithms)	Min	200	ns
t_{RH}	Reset# High Time Before Read	Min	50	ns
t_{RB1}	RY/BY# Recovery Time (to CE#, OE# go low)	Min	0	ns
t_{RB2}	RY/BY# Recovery Time (to WE# go low)	Min	50	ns
t_{READY1}	Reset# Pin Low (During Embedded Algorithms) to Read or Write	Max	20	us
t_{READY2}	Reset# Pin Low (NOT During Embedded Algorithms) to Read or Write	Max	500	ns

Figure 24. AC Waveforms for RESET# Reset# Timings



Reset Timing during Embedded Algorithms



Reset Timing NOT during Embedded Algorithms

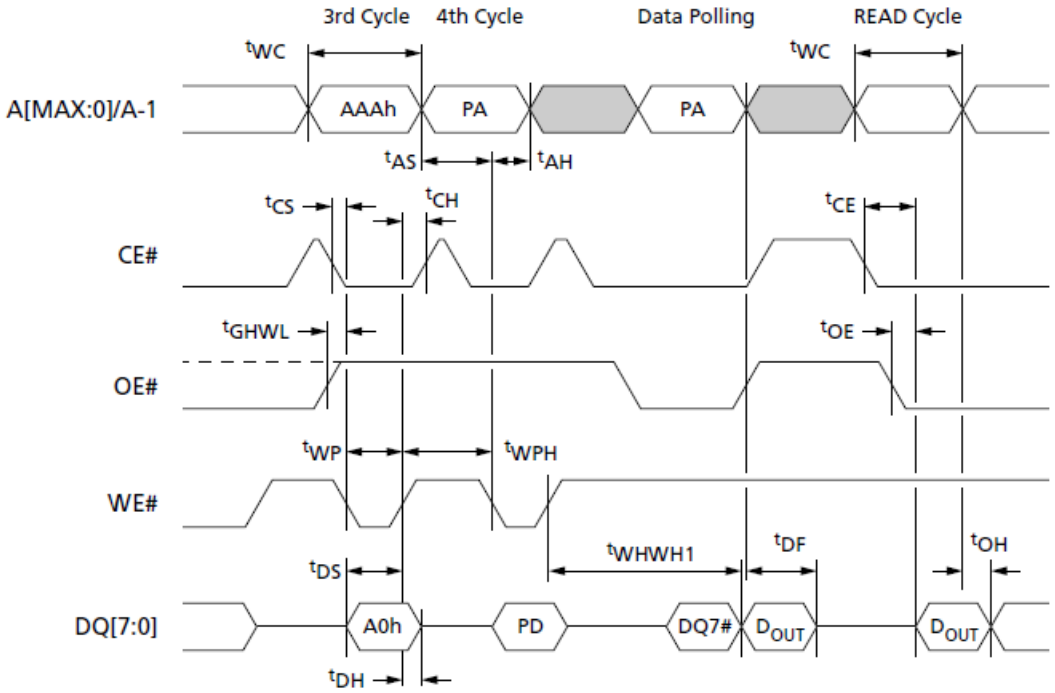
Write AC CHARACTERISTICS

Table 38. WE#-Controlled Write AC Characteristics

Parameter Symbols		Description	Condition	Package	Min	Max	Unit
JEDEC	Legacy						
t_{AVAV}	t_{WC}	Write Cycle Time	$V_{CCQ} \geq 2.7V$	BGA	60	-	ns
				TSOP	70	-	
			$V_{CCQ} \leq 2.7V$	BGA	65	-	ns
				TSOP	75	-	
t_{ELWL}	T_{CS}	CE# LOW to WE# LOW	-	BGA	0	-	ns
				TSOP	0	-	
t_{WLWH}	t_{WP}	WE# LOW to WE# HIGH	-	BGA	35	-	ns
				TSOP	35	-	
T_{DVWH}	T_{DS}	Input valid to WE# HIGH	-	BGA	30	-	ns
				TSOP	30	-	
T_{WHDX}	T_{DH}	WE# HIGH to input transition	-	BGA	0	-	ns
				TSOP	0	-	
T_{WHEH}	T_{CH}	WE# HIGH to CE# HIGH	-	BGA	0	-	ns
				TSOP	0	-	
T_{WHWL}	T_{WPH}	WE# HIGH to WE# LOW	-	BGA	20	-	ns
				TSOP	20	-	
T_{AVWL}	T_{AS}	Address valid to WE# LOW	-	BGA	0	-	ns
				TSOP	0	-	
T_{WLAX}	T_{AH}	WE# LOW to Address transition	-	BGA	45	-	ns
				TSOP	45	-	
T_{GHWL}	-	OE# HIGH to WE# LOW.	-	BGA	0	-	ns
				TSOP	0	-	
T_{WHGL}	T_{OEH}	WE# HIGH to OE# LOW.	-	BGA	0	-	us
				TSOP	0	-	
T_{WHRL}(1)	T_{BUSY}(1)	Program/erase valid to RY/BY# LOW	-	BGA	-	90	us
				TSOP	-	90	
T_{CHEL}	T_{VCS}	V_{CC} HIGH to CE# LOW	-	BGA	60	-	us
				TSOP	60	-	

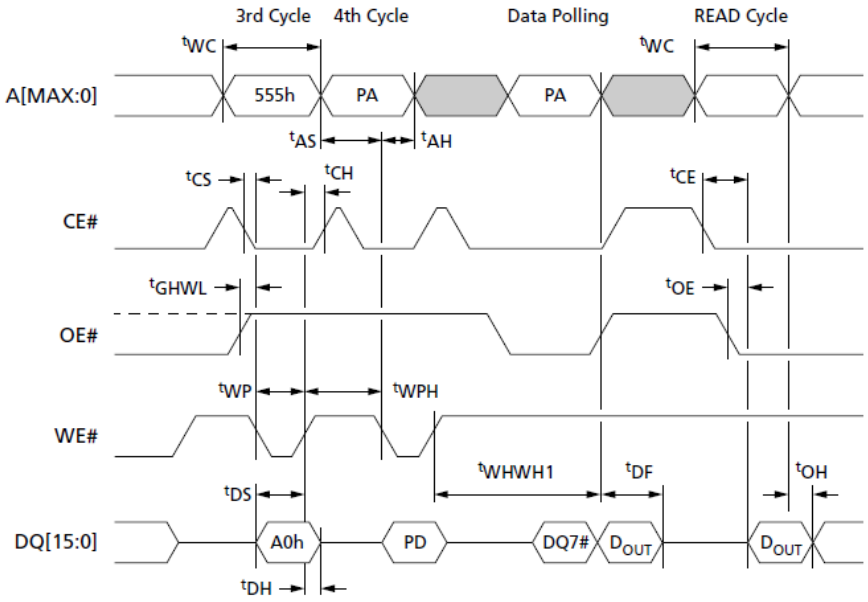
Note:
1. Sampled only; not 100% tested.

Figure 25. WE# Controlled Program AC Timing (x8 Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

Figure 26. WE# Controlled Program AC Timing (x16 Mode)

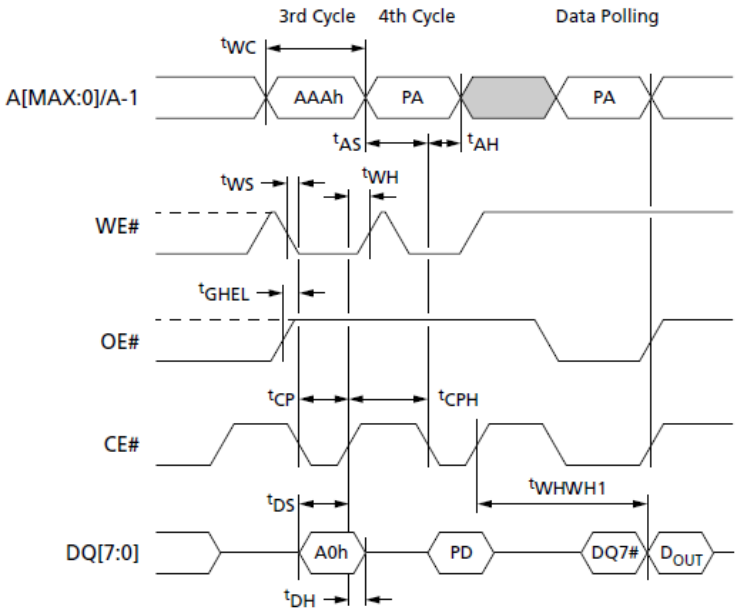


Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit and by a READ operation that outputs the data (D_{OUT}) programmed by the previous PROGRAM command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

Table 39. CE#-Controlled Write AC Characteristics

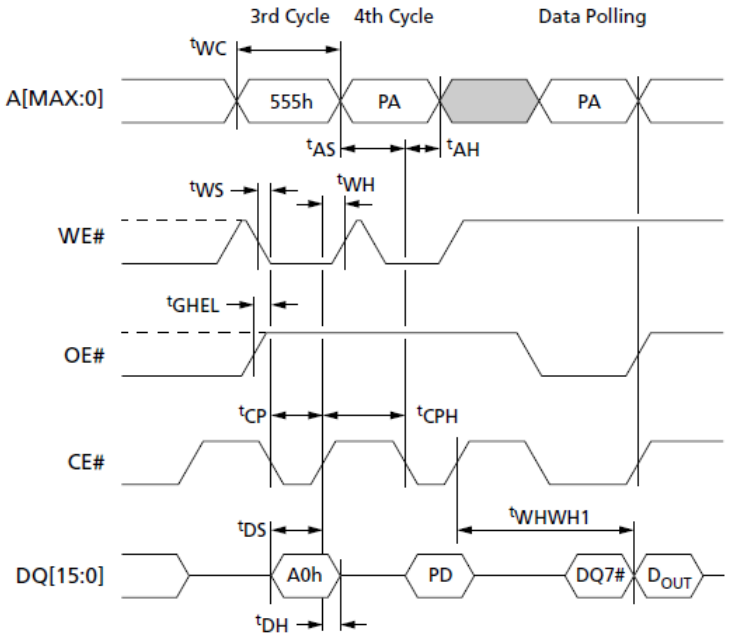
Parameter Symbols		Description	Condition	Package	Min	Max	Unit
JEDEC	Legacy						
t_{AVAV}	t_{WC}	Write Cycle Time	$V_{CCQ} \geq 2.7V$	BGA	60	-	ns
				TSOP	70	-	
			$V_{CCQ} \leq 2.7V$	BGA	65	-	ns
				TSOP	75	-	
T_{WLEL}	T_{WS}	WE# LOW to CE# LOW	-	BGA	0	-	ns
				TSOP	0	-	
T_{ELEH}	T_{CP}	CE# LOW to CE# HIGH	-	BGA	35	-	ns
				TSOP	35	-	
T_{DVEH}	T_{DS}	Input valid to CE# HIGH	-	BGA	30	-	ns
				TSOP	30	-	
T_{EHDX}	T_{DH}	CE# HIGH to input transition	-	BGA	0	-	ns
				TSOP	0	-	
T_{EHWH}	T_{WH}	CE# HIGH to WE# HIGH	-	BGA	0	-	ns
				TSOP	0	-	
T_{EHEL}	T_{CPH}	CE# HIGH to CE# HIGH	-	BGA	20	-	ns
				TSOP	20	-	
T_{AVEL}	T_{AS}	Address valid to CE# LOW	-	BGA	0	-	ns
				TSOP	0	-	
T_{ELAX}	T_{AH}	CE# LOW to Address transition	-	BGA	45	-	ns
				TSOP	45	-	
T_{GHEL}	-	OE# HIGH to CE# LOW.	-	BGA	0	-	ns
				TSOP	0	-	

Figure 27. CE# Controlled Program AC Timing (x8 Mode)



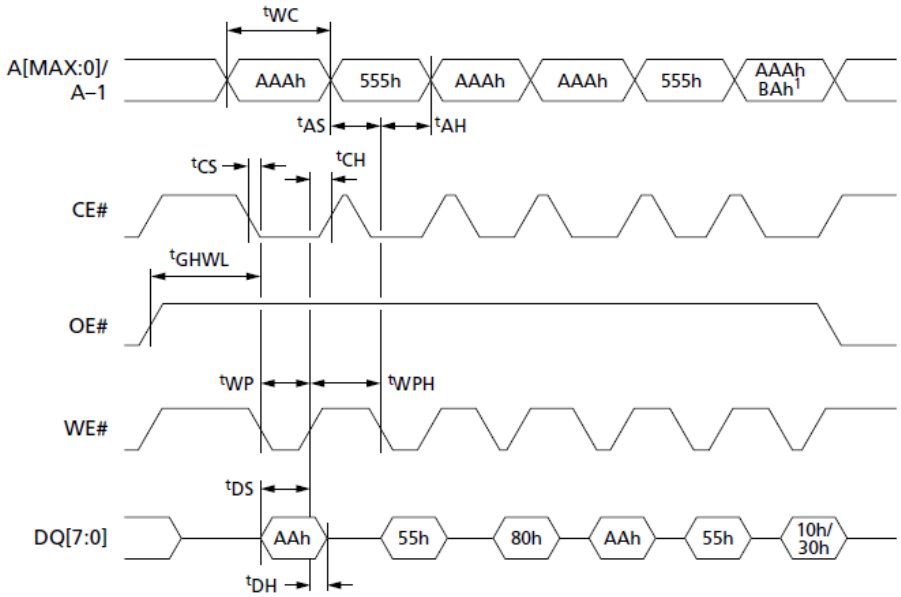
Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

Figure 28. CE# Controlled Program AC Timing (x16 Mode)



Notes:
1. Only the third and fourth cycles of the PROGRAM command are represented. The PROGRAM command is followed by checking of the status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7. (See Data Polling Bit [DQ7].)
4. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

Figure 29. CE# Controlled Program AC Timing (x16 Mode)



Notes:
1. For a CHIP ERASE command, the address is 555h, and the data is 10h; for a BLOCK ERASE command, the address is BAd, and the data is 30h.
2. BAd is the block address.
3. See the following tables for timing details: Read AC Characteristics, WE#-Controlled Write AC Characteristics, and CE#-Controlled Write AC Characteristics.

Accelerated Program, Data Polling/Toggle AC Characteristics

Table 40. Accelerated Program and Data Polling/Data Toggle AC Characteristics

Parameter Symbols		Description	Min	Max	Unit
JEDEC	Legacy				
T_{VHVPP}	-	Vpp/WP# rising or falling time	250	-	ns
T_{VHHWH}	-	Valid V_{HH} on Vpp/WP# to WE# HIGH	50	-	ns
T_{AXGL}	T_{ASO}	Address setup time to OE# LOW during toggle bit polling	15	-	ns
T_{GHAX}, T_{EHAX}	T_{AHT}	Address hold time from OE# during toggle bit polling	0	-	ns
T_{EHEL2}	T_{EPH}	CE# HIGH during toggle bit polling	20	-	ns
T_{WHGL2}, T_{GHGL2}	T_{OEH}	Output hold time during data and toggle bit polling	20	-	ns
T_{WHRL}	T_{BUSY}	Program/erase valid to RY#/BY# LOW	-	90	ns

Note: 1. Sampled only; not 100% tested.

Figure 30. Accelerated Program AC Timing

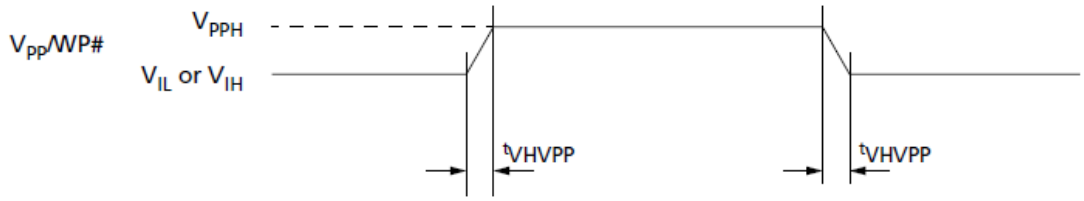
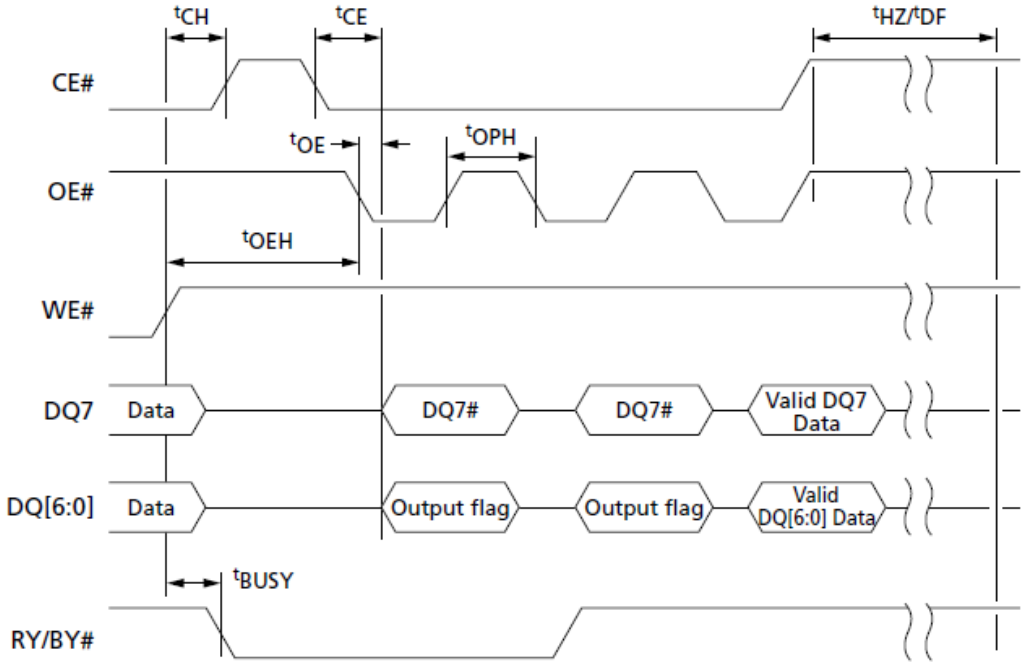


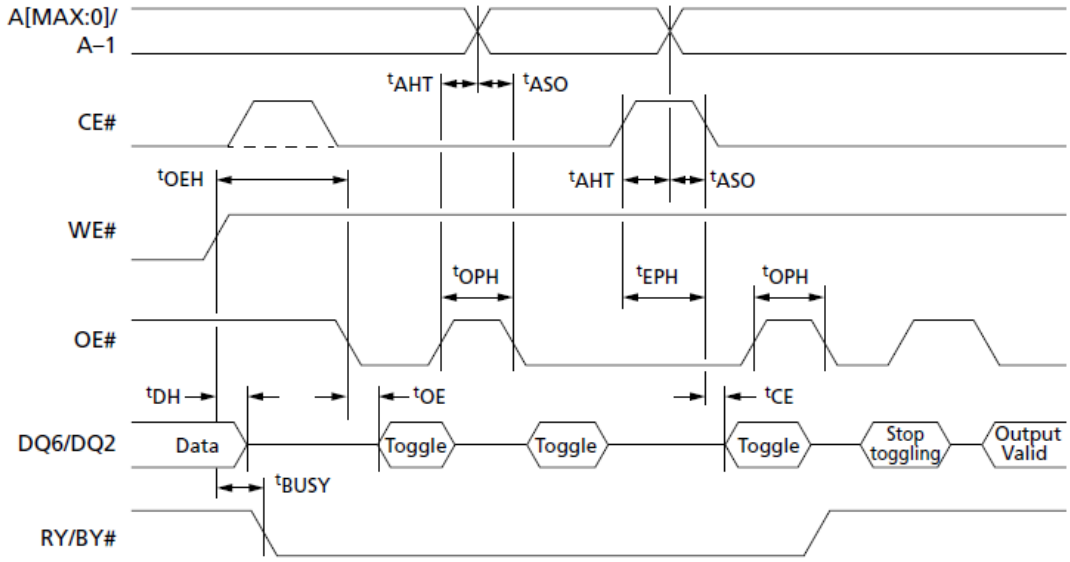
Figure 31. Data Polling AC Timing



Note:

1. DQ7 returns a valid data bit when the PROGRAM or ERASE command has completed.

Figure 32. Toggle/Alternative Toggle Bit Polling AC Timing (x8 Mode)



Notes:

1. DQ6 stops toggling when the PROGRAM or ERASE command has completed. DQ2 stops toggling when the CHIP ERASE or BLOCK ERASE command has completed.

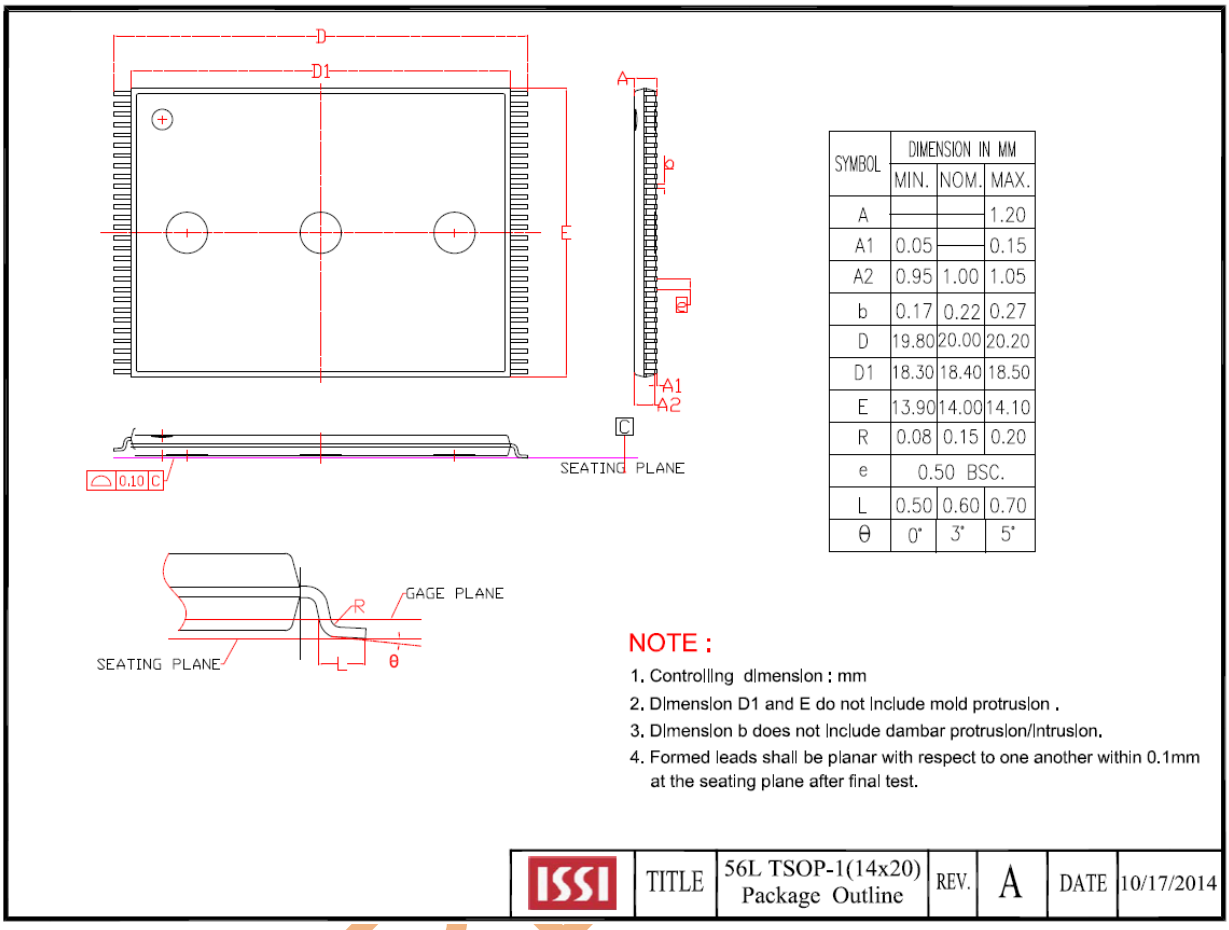
Accelerated Program, Data Polling/Toggle AC Characteristics

Table 41. Program/Erase Characteristics

Parameter		Buffer Size	Byte	Word	Min	Typ (1,2)	Max(2)	Unit
Block Erase		-	-	-		0.5	4	s
Erase suspend latency		-	-	-		20	25	us
Block erase timeout					50	-		us
Byte program	Single-byte program	-	-	-	-	15	175	us
	Double-/ Quardruple-/ Octuple-byte program	-	-	-	-	10	200	us
	Byte Write to buffer program	32B	32	-	-	80	250	us
		64B	64	-	-	160	500	us
		256B	256	-	-	640	2000	us
Word program	Single-word program	-	-	-	-	15	175	us
	Word write to buffer program	16W	-	16	-	80	250	us
		32W	-	32	-	160	500	us
		128W	-	128	-	640	2000	us
		256W	-	256	-	1280	4000	us
	Full buffer program with V_{PPH}	256	-	256	-	480	1200	us
	Effective write to buffer program per word	16	-	1	-	5	15.6	us
		32	-	1	-	5	15.6	us
		128	-	1	-	5	15.6	us
		256	-	1	-	5	15.6	us
	Effective full buffer program per word with V_{PPH}	256	-	1	-	1.9	4.7	us
Program suspend latency		-	-	-	-	20	25	us
Blank check		-	-	-	-	20	-	ms
PROGRAM/ERASE cycles (per block)		-	-		100,000	-	-	cycles

Notes:
1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.

FIGURE 33. 56-pin TSOP 14mmx20mm package outline



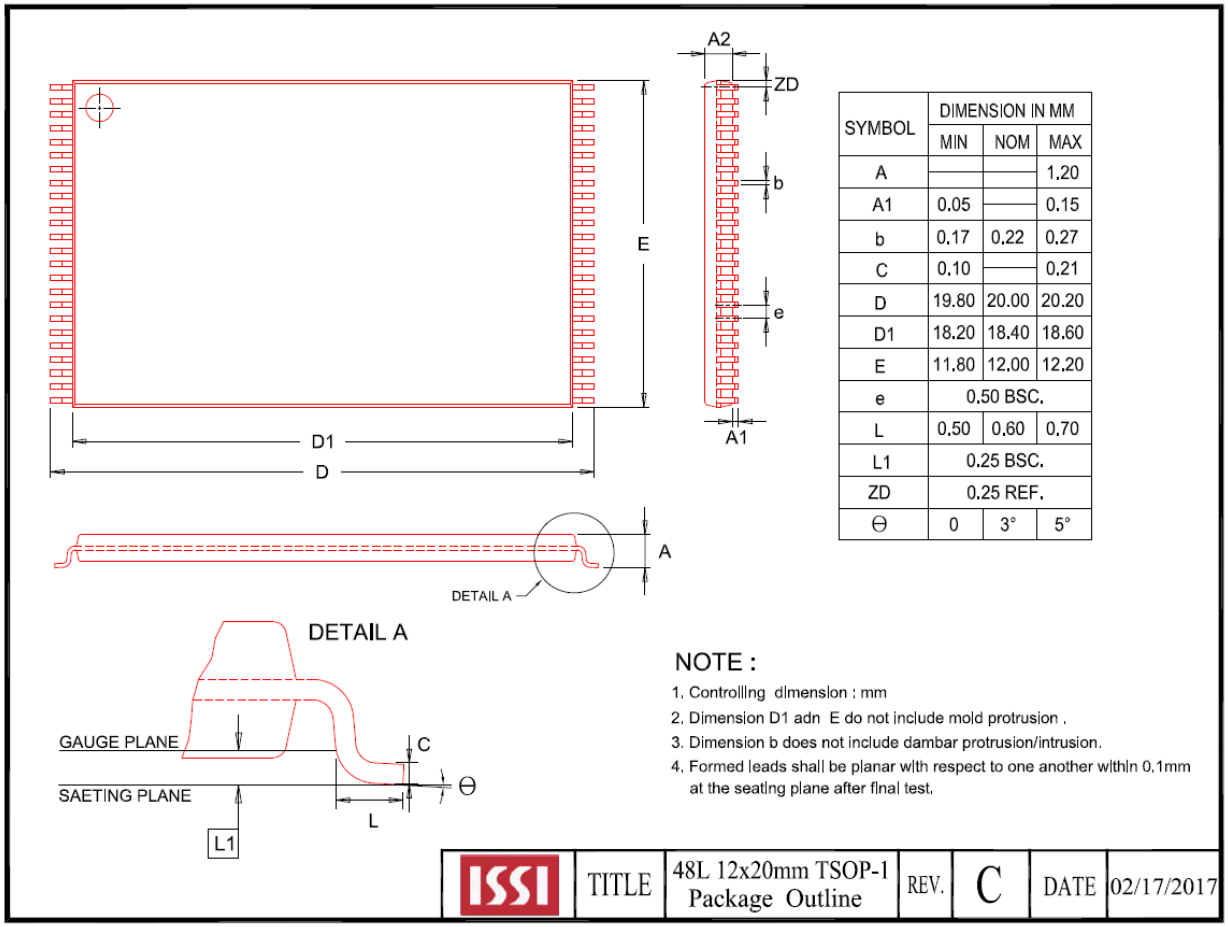
SYMBOL	DIMENSION IN MM		
	MIN.	NOM.	MAX.
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	13.90	14.00	14.10
R	0.08	0.15	0.20
e	0.50 BSC.		
L	0.50	0.60	0.70
θ	0°	3°	5°

NOTE :

1. Controlling dimension : mm
2. Dimension D1 and E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

ISSI	TITLE	56L TSOP-1(14x20) Package Outline	REV.	A	DATE	10/17/2014

FIGURE 34. 48-pin TSOP 12mmx20mm package outline



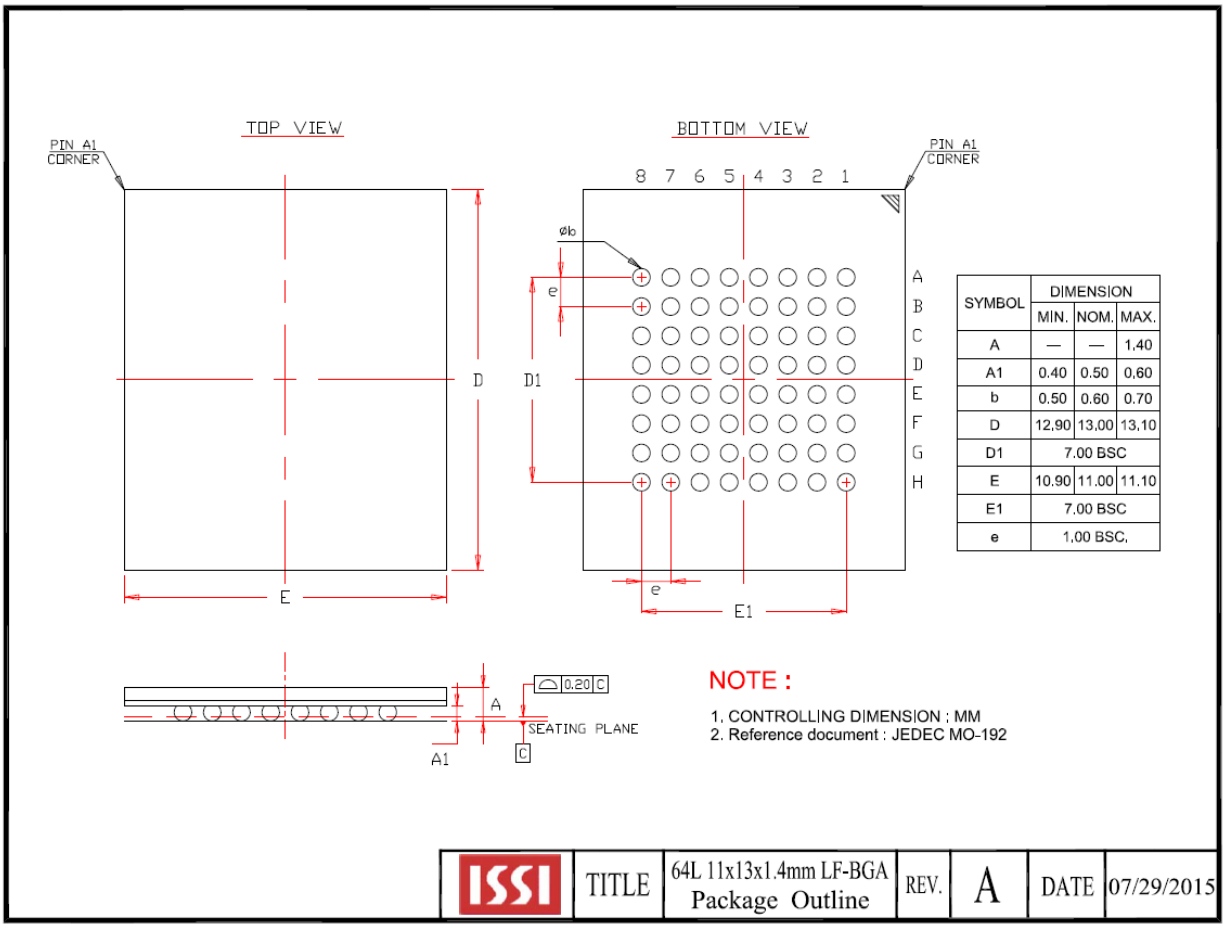
SYMBOL	DIMENSION IN MM		
	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
b	0.17	0.22	0.27
C	0.10		0.21
D	19.80	20.00	20.20
D1	18.20	18.40	18.60
E	11.80	12.00	12.20
e	0.50 BSC.		
L	0.50	0.60	0.70
L1	0.25 BSC.		
ZD	0.25 REF.		
Θ	0	3°	5°

NOTE :

1. Controlling dimension : mm
2. Dimension D1 adn E do not include mold protrusion .
3. Dimension b does not include dambar protrusion/intrusion.
4. Formed leads shall be planar with respect to one another within 0.1mm at the seating plane after final test.

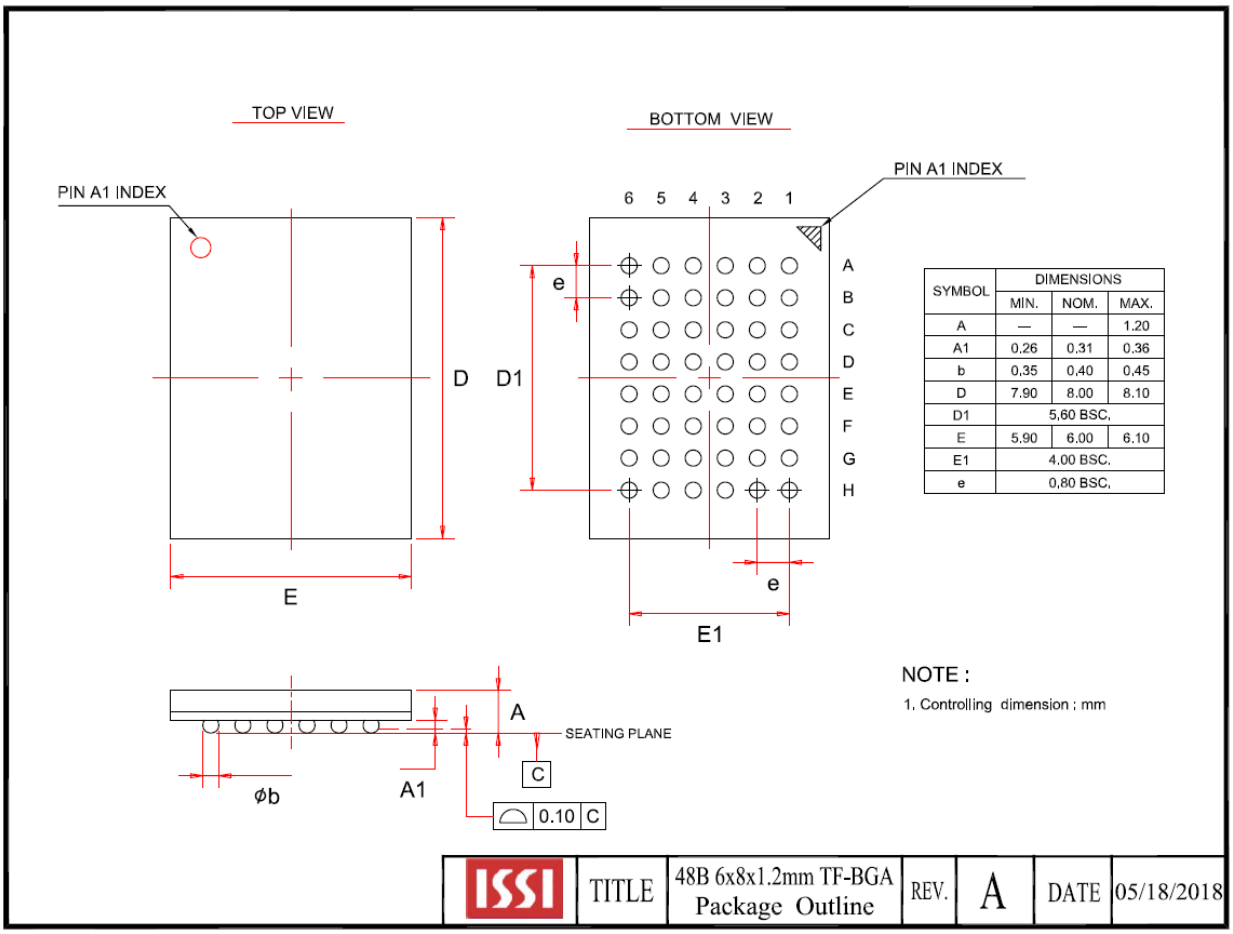
	TITLE	48L 12x20mm TSOP-1 Package Outline	REV.	C	DATE	02/17/2017

FIGURE 35. 64-ball Ball Grid Array (BGA), 11x13 mm, Pitch 1mm package outline



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.40
A1	0.40	0.50	0.60
b	0.50	0.60	0.70
D	12.90	13.00	13.10
D1		7.00 BSC	
E	10.90	11.00	11.10
E1		7.00 BSC	
e		1.00 BSC.	

FIGURE 36. 48-ball Ball Grid Array (BGA), 6x8x1.2mm, Pitch 0.8mm package outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.26	0.31	0.36
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1		5.60 BSC.	
E	5.90	6.00	6.10
E1		4.00 BSC.	
e		0.80 BSC.	

ORDERING INFORMATION

IS29GL 064 - 60 T L E T

SECTOR for WRITE PROTECT (WP#/ACC=L)
T = Highest block protected, uniform block by Vpp/WP#
B = Lowest block protected, uniform block by Vpp/WP#
U = Top boot; top two blocks protected by Vpp/WP#
D= Bottom boot; bottom two blocks protected by Vpp/WP#

TEMPERATURE RANGE
E = Extended Grade (-40°C to +105°C)
A3 = Automotive Grade (-40°C to +125°C)

PACKAGING CONTENT
L = RoHS compliant

PACKAGE
S = 56-pin TSOP
T = 48-pin TSOP
F = 64-ball BGA 1.0mm pitch, 11mm x 13mm
B = 48-ball BGA 0.8mm pitch, 6mm x 8mm
W = KGD (Call Factory)

SPEED at VCCQ=2.7~3.6V.
60 = 60ns
70 = 70ns

Density
064 = 128 Mb (8M x 8 / 4M x 16)
032 = 32 Mb (4M x 8 / 2M x 16)
016 = 16 Mb (42M x 8 / 1M x 16)

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.
29GL = FLASH, 3V Page Mode Flash Memory

64Mb

Temperature	Order Part Number	Block Protection[2]	Package
Extended (-40°C to +105°C)	IS29GL064-70SLET	Highest Block, Uniform block	56-pin TSOP
	IS29GL064-70SLEB	Lowest Block, Uniform block	
	IS29GL064-70SLEU	Top Two Block, Top Boot	
	IS29GL064-70SLED	Bottom Two Block, Bottom Boot	
	IS29GL064-70TLET	Highest Block, Uniform block	48-pin TSOP
	IS29GL064-70TLEB	Lowest Block, Uniform block	
	IS29GL064-70TLEU	Top Two Block, Top Boot	
	IS29GL064-70TLED	Bottom Two Block, Bottom Boot	
	IS29GL064-60FLET	Highest Block, Uniform block	64-ball BGA (11x13mm)
	IS29GL064-60FLEB	Lowest Block, Uniform block	
	IS29GL064-60FLEU	Top Two Block, Top Boot	
	IS29GL064-60FLED	Bottom Two Block, Bottom Boot	
	IS29GL064-60BLET	Highest Block, Uniform block	48-ball BGA (6x8mm)
	IS29GL064-60BLEB	Lowest Block, Uniform block	
	IS29GL064-60BLEU	Top Two Block, Top Boot	
	IS29GL064-60BLED	Bottom Two Block, Bottom Boot	
Automotive. A3 (-40°C to +125°C)	IS29GL064-70SLA3T	Highest Block, Uniform block	56-pin TSOP
	IS29GL064-70SLA3B	Lowest Block, Uniform block	
	IS29GL064-70SLA3U	Top Two Block, Top Boot	
	IS29GL064-70SLA3D	Bottom Two Block, Bottom Boot	
	IS29GL064-70TLA3T	Highest Block, Uniform block	48-pin TSOP
	IS29GL064-70TLA3B	Lowest Block, Uniform block	
	IS29GL064-70TLA3U	Top Two Block, Top Boot	
	IS29GL064-70TLA3D	Bottom Two Block, Bottom Boot	
	IS29GL064-60FLA3T	Highest Block, Uniform block	64-ball BGA (11x13mm)
	IS29GL064-60FLA3B	Lowest Block, Uniform block	
	IS29GL064-60FLA3U	Top Two Block, Top Boot	
	IS29GL064-60FLA3D	Bottom Two Block, Bottom Boot	
	IS29GL064-60BLA3T	Highest Block, Uniform block	48-ball BGA (6x8mm)
	IS29GL064-60BLA3B	Lowest Block, Uniform block	
	IS29GL064-60BLA3U	Top Two Block, Top Boot	
	IS29GL064-60BLA3D	Bottom Two Block, Bottom Boot	

32Mb

Temperature	Order Part Number	Block Protection[2]	Package
Extended (-40°C to +105°C)	IS29GL032-70SLET	Highest Block, Uniform block	56-pin TSOP
	IS29GL032-70SLEB	Lowest Block, Uniform block	
	IS29GL032-70SLEU	Top Two Block, Top Boot	
	IS29GL032-70SLED	Bottom Two Block, Bottom Boot	
	IS29GL032-70TLET	Highest Block, Uniform block	48-pin TSOP
	IS29GL032-70TLEB	Lowest Block, Uniform block	
	IS29GL032-70TLEU	Top Two Block, Top Boot	
	IS29GL032-70TLED	Bottom Two Block, Bottom Boot	
	IS29GL032-60FLET	Highest Block, Uniform block	64-ball BGA (11x13mm)
	IS29GL032-60FLEB	Lowest Block, Uniform block	
	IS29GL032-60FLEU	Top Two Block, Top Boot	
	IS29GL032-60FLED	Bottom Two Block, Bottom Boot	
	IS29GL032-60BLET	Highest Block, Uniform block	48-ball BGA (6x8mm)
	IS29GL032-60BLEB	Lowest Block, Uniform block	
	IS29GL032-60BLEU	Top Two Block, Top Boot	
	IS29GL032-60BLED	Bottom Two Block, Bottom Boot	
Automotive. A3 (-40°C to +125°C)	IS29GL032-80SLA3T	Highest Block, Uniform block	56-pin TSOP
	IS29GL032-80SLA3B	Lowest Block, Uniform block	
	IS29GL032-80SLA3U	Top Two Block, Top Boot	
	IS29GL032-80SLA3D	Bottom Two Block, Bottom Boot	
	IS29GL032-80TLA3T	Highest Block, Uniform block	48-pin TSOP
	IS29GL032-80TLA3B	Lowest Block, Uniform block	
	IS29GL032-80TLA3U	Top Two Block, Top Boot	
	IS29GL032-80TLA3D	Bottom Two Block, Bottom Boot	
	IS29GL032-70FLA3T	Highest Block, Uniform block	64-ball BGA (11x13mm)
	IS29GL032-70FLA3B	Lowest Block, Uniform block	
	IS29GL032-70FLA3U	Top Two Block, Top Boot	
	IS29GL032-70FLA3D	Bottom Two Block, Bottom Boot	
	IS29GL032-70BLA3T	Highest Block, Uniform block	48-ball BGA (6x8mm)
	IS29GL032-70BLA3B	Lowest Block, Uniform block	
	IS29GL032-70BLA3U	Top Two Block, Top Boot	
	IS29GL032-70BLA3D	Bottom Two Block, Bottom Boot	

16Mb

Temperature	Order Part Number	Block Protection[2]	Package
Extended (-40°C to +105°C)	IS29GL016-70SLET	Highest Block, Uniform block	56-pin TSOP
	IS29GL016-70SLEB	Lowest Block, Uniform block	
	IS29GL016-70SLEU	Top Two Block, Top Boot	
	IS29GL016-70SLED	Bottom Two Block, Bottom Boot	
	IS29GL016-70TLET	Highest Block, Uniform block	48-pin TSOP
	IS29GL016-70TLEB	Lowest Block, Uniform block	
	IS29GL016-70TLEU	Top Two Block, Top Boot	
	IS29GL016-70TLED	Bottom Two Block, Bottom Boot	
	IS29GL016-60FLET	Highest Block, Uniform block	64-ball BGA (11x13mm)
	IS29GL016-60FLEB	Lowest Block, Uniform block	
	IS29GL016-60FLEU	Top Two Block, Top Boot	
	IS29GL016-60FLED	Bottom Two Block, Bottom Boot	
	IS29GL016-60BLET	Highest Block, Uniform block	48-ball BGA (6x8mm)
	IS29GL016-60BLEB	Lowest Block, Uniform block	
	IS29GL016-60BLEU	Top Two Block, Top Boot	
	IS29GL016-60BLED	Bottom Two Block, Bottom Boot	
Automotive. A3 Temp. (-40°C to +125°C)	IS29GL016-70SLA3T	Highest Block, Uniform block	56-pin TSOP
	IS29GL016-70SLA3B	Lowest Block, Uniform block	
	IS29GL016-70SLA3U	Top Two Block, Top Boot	
	IS29GL016-70SLA3D	Bottom Two Block, Bottom Boot	
	IS29GL016-70TLA3T	Highest Block, Uniform block	48-pin TSOP
	IS29GL016-70TLA3B	Lowest Block, Uniform block	
	IS29GL016-70TLA3U	Top Two Block, Top Boot	
	IS29GL016-70TLA3D	Bottom Two Block, Bottom Boot	
	IS29GL016-60FLA3T	Highest Block, Uniform block	64-ball BGA (11x13mm)
	IS29GL016-60FLA3B	Lowest Block, Uniform block	
	IS29GL016-60FLA3U	Top Two Block, Top Boot	
	IS29GL016-60FLA3D	Bottom Two Block, Bottom Boot	
	IS29GL016-60BLA3T	Highest Block, Uniform block	48-ball BGA (6x8mm)
	IS29GL016-60BLA3B	Lowest Block, Uniform block	
	IS29GL016-60BLA3U	Top Two Block, Top Boot	
	IS29GL016-60BLA3D	Bottom Two Block, Bottom Boot	

Notes:
1. A3: Meet AEC-Q100 requirements with PPAP
Temp Grades: E= -40 to 105ºC, A3= -40 to 125ºC
2. WP#/ACC=L