



RLDRAM 3

ADVANCED INFORMATION

IS49RL18128– 4 Meg x 18 x 16 Banks x 2 Ranks

IS49RL36640– 2Meg x 36 x 16 Banks

Features

- The 2Gb (DDP:Dual Die Package) RLDRAM 3 uses ISSI's 1Gb RLDRAM 3 die.
- 933 MHz DDR operation (1866 Mb/s/ball data rate)
- Organization
 - 128 Meg x 18, and 64 Meg x 36 common I/O
 - 16 banks
- 1.2V center-terminated push/pull I/O
- 2.5V V_{EXT} , 1.35V V_{DD} , 1.2V V_{DDQ} (optional 1.35V V_{DDQ} for 1866 operation only).
- Reduced cycle time ($t_{RC} (MIN) = 8ns$)
- SDR addressing
- Programmable READ/WRITE latency (RL/WL) and burst length
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Free-running differential input data clocks (DK x, DK x#) and output data clocks (QK x, QK x#)
- On-die DLL generates CK edge-aligned data and differential output data clock signals
- 64ms refresh (128K refresh per 64ms)
- 40 Ω or 60 Ω matched impedance outputs
- Integrated on-die termination (ODT)
- Single or multibank writes
- Extended operating range (200–933 MHz)
- READ training register
- Multiplexed and non-multiplexed addressing capabilities
- Mirror function
- Output driver and ODT calibration
- Post Package Repair - 1 row per half bank
- JTAG interface (IEEE 1149.1-2001)

Options

- Clock cycle and t_{RC} timing
 - 1.07 ns and $t_{RC} (MIN) = 8ns$ (RL3-1866) for -107E
 - 1.25ns and $t_{RC} (MIN) = 10ns$ (RL3-1600) for -125E
 - 1.25ns and $t_{RC} (MIN) = 12ns$ (RL3-1600) for -125
- Configuration
 - 128 Meg x 18
 - 64 Meg x 36

Operating Temperature

- – Commercial ($T_C = 0^\circ$ to $+95^\circ C$)
- Industrial ($T_C = -40^\circ C$ to $+95^\circ C$)

Package

- – 168-ball LFBGA (Pb-free) ,13.5mm x 13.5mm x 1.4mm

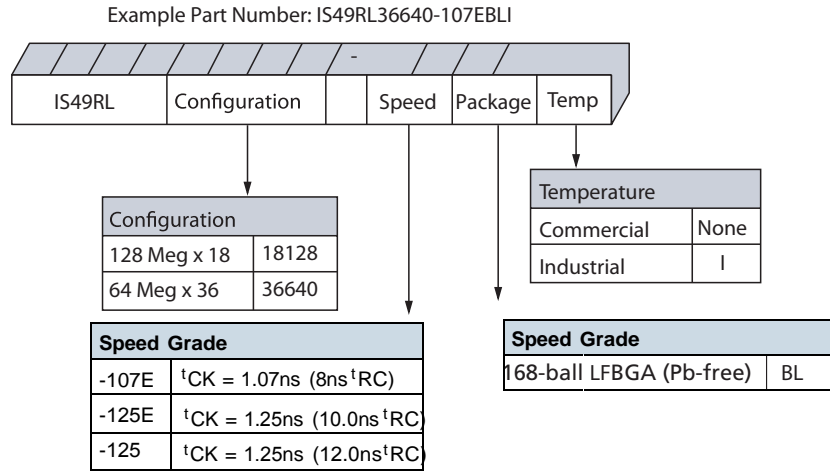
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Figure 1: 2Gb RLDRAM® 3 Part Numbers





Ball Assignments and Descriptions

Table 1: 128 Meg x 18 Ball Assignments – 168-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V _{SS}	V _{DD}	NF	V _{DDQ}	NF	V _{REF}	DQ7	V _{DDQ}	DQ8	V _{DD}	V _{SS}	RESET#
B	V _{EXT}	V _{SS}	NF	V _{SSQ}	NF	V _{DDQ}	DM0	V _{DDQ}	DQ5	V _{SSQ}	DQ6	V _{SS}	V _{EXT}
C	V _{DD}	NF	V _{DDQ}	NF	V _{SSQ}	NF	DK0#	DQ2	V _{SSQ}	DQ3	V _{DDQ}	DQ4	V _{DD}
D	A11	V _{SSQ}	NF	V _{DDQ}	NF	V _{SSQ}	DK0	V _{SSQ}	QK0	V _{DDQ}	DQ0	V _{SSQ}	A13
E	V _{SS}	A0	V _{SSQ}	NF	V _{DDQ}	NF	MF	QK0#	V _{DDQ}	DQ1	V _{SSQ}	CS#	V _{SS}
F	A7	A20	V _{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V _{DD}	A5	A9
G	RFU	A15	A6	V _{SS}	BA1	V _{SS}	CK#	V _{SS}	BA0	V _{SS}	A8	A18	CS1#
H	A19	V _{DD}	A14	A16	V _{DD}	BA3	CK	BA2	V _{DD}	A17	A12	V _{DD}	A10
J	V _{DDQ}	NF	V _{SSQ}	NF	V _{DDQ}	NF	V _{SS}	QK1#	V _{DDQ}	DQ9	V _{SSQ}	QVLD	V _{DDQ}
K	NF	V _{SSQ}	NF	V _{DDQ}	NF	V _{SSQ}	DK1	V _{SSQ}	QK1	V _{DDQ}	DQ10	V _{SSQ}	DQ11
L	V _{DD}	NF	V _{DDQ}	NF	V _{SSQ}	NF	DK1#	DQ12	V _{SSQ}	DQ13	V _{DDQ}	DQ14	V _{DD}
M	V _{EXT}	V _{SS}	NF	V _{SSQ}	NF	V _{DDQ}	DM1	V _{DDQ}	DQ15	V _{SSQ}	DQ16	V _{SS}	V _{EXT}
N	V _{SS}	TCK	V _{DD}	TDO	V _{DDQ}	NF	V _{REF}	DQ17	V _{DDQ}	TDI	V _{DD}	TMS	V _{SS}

Notes:

1. NF balls for the x18 configuration are internally connected and have parasitic characteristics of an I/O. Balls may be connected to V_{SSQ}.
2. MF is assumed to be tied LOW for this ball assignment.



Table 1: 64 Meg x 36 Ball Assignments – 168-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V _{SS}	V _{DD}	DQ26	V _{DDQ}	DQ25	V _{REF}	DQ7	V _{DDQ}	DQ8	V _{DD}	V _{SS}	RESET#
B	V _{EXT}	V _{SS}	DQ24	V _{SSQ}	DQ23	V _{DDQ}	DM0	V _{DDQ}	DQ5	V _{SSQ}	DQ6	V _{SS}	V _{EXT}
C	V _{DD}	DQ22	V _{DDQ}	DQ21	V _{SSQ}	DQ20	DK0#	DQ2	V _{SSQ}	DQ3	V _{DDQ}	DQ4	V _{DD}
D	A11	V _{SSQ}	DQ18	V _{DDQ}	QK2	V _{SSQ}	DK0	V _{SSQ}	QK0	V _{DDQ}	DQ0	V _{SSQ}	A13
E	V _{SS}	A0	V _{SSQ}	DQ19	V _{DDQ}	QK2#	MF	QK0#	V _{DDQ}	DQ1	V _{SSQ}	CS#	V _{SS}
F	A7	A20	V _{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V _{DD}	A5	A9
G	V _{SS}	A15	A6	V _{SS}	BA1	V _{SS}	CK#	V _{SS}	BA0	V _{SS}	A8	A18	V _{SS}
H	A19	V _{DD}	A14	A16	V _{DD}	BA3	CK	BA2	V _{DD}	A17	A12	V _{DD}	A10
J	V _{DDQ}	QVLD1	V _{SSQ}	DQ27	V _{DDQ}	QK3#	V _{SS}	QK1#	V _{DDQ}	DQ9	V _{SSQ}	QVLD0	V _{DDQ}
K	DQ29	V _{SSQ}	DQ28	V _{DDQ}	QK3	V _{SSQ}	DK1	V _{SSQ}	QK1	V _{DDQ}	DQ10	V _{SSQ}	DQ11
L	V _{DD}	DQ32	V _{DDQ}	DQ31	V _{SSQ}	DQ30	DK1#	DQ12	V _{SSQ}	DQ13	V _{DDQ}	DQ14	V _{DD}
M	V _{EXT}	V _{SS}	DQ34	V _{SSQ}	DQ33	V _{DDQ}	DM1	V _{DDQ}	DQ15	V _{SSQ}	DQ16	V _{SS}	V _{EXT}
N	V _{SS}	TCK	V _{DD}	TDO	V _{DDQ}	DQ35	V _{REF}	DQ17	V _{DDQ}	TDI	V _{DD}	TMS	V _{SS}

Notes:

1. NF ball for x36 configuration is internally connected and has parasitic characteristics of an address. Ball may be connected to V_{SSQ}.
2. MF is assumed to be tied LOW for this ball assignment.



Ordering Information

Commercial Range: $T_C = 0^{\circ}\text{C}$ to $+95^{\circ}\text{C}$

Frequency	Speed (tCK)	tRC(min)	Order Part No.	Organization	Package
933MHz	1.07ns	8.0ns	IS49RL18128-107EBL	128M x 18	168 LFBGA, Lead-free
			IS49RL36640-107EBL	64M x 36	
800MHz	1.25ns	10.0ns	IS49RL18128-125EBL	128M x 18	
			IS49RL36640-125EBL	64M x 36	
		12.0ns	IS49RL18128-125BL	128M x 18	
			IS49RL36640-125BL	64M x 36	

Industrial Range: $T_C = -40^{\circ}\text{C}$ to $+95^{\circ}\text{C}$

Frequency	Speed (tCK)	tRC(min)	Order Part No.	Organization	Package
933MHz	1.07ns	8.0ns	IS49RL18128-107EBLI	128M x 18	168 LFBGA, Lead-free
			IS49RL36640-107EBLI	64M x 36	
800MHz	1.25ns	10.0ns	IS49RL18128-125EBLI	128M x 18	
			IS49RL36640-125EBLI	64M x 36	
		12.0ns	IS49RL18128-125BLI	128M x 18	
			IS49RL36640-125BLI	64M x 36	

168-Ball LFBGA Package drawing – 13.5x13.5x1.4mm BGA

