RLDRAM 3

ADVANCED INFORMATION

IS49RL18128– 4 Meg x 18 x 16 Banks x 2 Ranks
IS49RL36640– 2Meg x 36 x 16 Banks

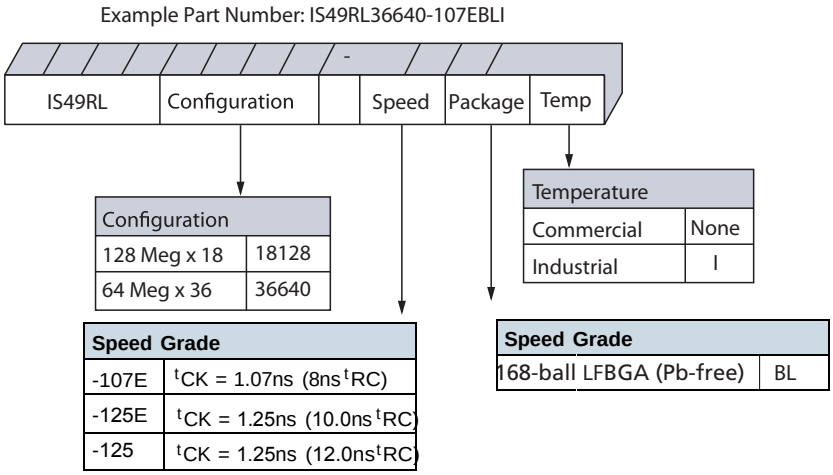
Features

- The 2Gb (DDP:Dual Die Package) RLDRAM 3 uses ISSI's 1Gb RLDRAM 3 die.
- 933 MHz DDR operation (1866 Mb/s/ball data rate)
- Organization
  - 128 Meg x 18, and 64 Meg x 36 common I/O
  - 16 banks
- 1.2V center-terminated push/pull I/O
- 2.5V V_{EXT}, 1.35V V_{DD}, 1.2V V_{DDQ} (optional 1.35V V_{DDQ} for 1866 operation only).
- Reduced cycle time (^{t}RC (MIN) = 8ns)
- SDR addressing
- Programmable READ/WRITE latency (RL/WL) and burst length
- Data mask for WRITE commands
- Differential input clocks (CK, CK#)
- Free-running differential input data clocks (DK x, DK x#) and output data clocks (QK x, QK x#)
- On-die DLL generates CK edge-aligned data and differential output data clock signals
- 64ms refresh (128K refresh per 64ms)
- 40 Ω or 60 Ω matched impedance outputs
- Integrated on-die termination (ODT)
- Single or multibank writes
- Extended operating range (200–933 MHz)
- READ training register
- Multiplexed and non-multiplexed addressing capabilities
- Mirror function
- Output driver and ODT calibration
- Post Package Repar - 1 row per half bank
- JTAG interface (IEEE 1149.1-2001)

Options

- Clock cycle and ^{t}RC timing
  - 1.07 ns and ^{t}RC (MIN) = 8ns (RL3-1866) for -107E
  - 1.25ns and ^{t}RC (MIN) = 10ns (RL3-1600) for -125E
  - 1.25ns and ^{t}RC (MIN) = 12ns (RL3-1600) for -125
- Configuration
  - -128 Meg x 18
  - - 64 Meg x 36
- Operating Temperature
  - Commercial (T_C = 0° to +95°C)
  - Industrial (T_C = –40°C to +95°C)
- Package
  - 168-ball LFBGA (Pb-free) ,13.5mm x 13.5mm x 1.4mm

Figure 1: 2Gb RLDRAM® 3 Part Numbers



Ball Assignments and Descriptions

Table 1: 128 Meg x 18 Ball Assignments – 168-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	NF	V_{DDQ}	NF	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	NF	V_{DDQ}	NF	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
F	A7	A20	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	RFU	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	CS1#
H	A19	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD	V_{DDQ}
K	NF	V_{SSQ}	NF	V_{DDQ}	NF	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	NF	V_{DDQ}	NF	V_{SSQ}	NF	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	NF	V_{SSQ}	NF	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	NF	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes:

1. NF balls for the x18 configuration are internally connected and have parasitic characteristics of an I/O. Balls may be connected to V_{SSQ}.
2. MF is assumed to be tied LOW for this ball assignment.

Table 1: 64 Meg x 36 Ball Assignments – 168-Ball BGA (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		V_{SS}	V_{DD}	DQ26	V_{DDQ}	DQ25	V_{REF}	DQ7	V_{DDQ}	DQ8	V_{DD}	V_{SS}	RESET#
B	V_{EXT}	V_{SS}	DQ24	V_{SSQ}	DQ23	V_{DDQ}	DM0	V_{DDQ}	DQ5	V_{SSQ}	DQ6	V_{SS}	V_{EXT}
C	V_{DD}	DQ22	V_{DDQ}	DQ21	V_{SSQ}	DQ20	DK0#	DQ2	V_{SSQ}	DQ3	V_{DDQ}	DQ4	V_{DD}
D	A11	V_{SSQ}	DQ18	V_{DDQ}	QK2	V_{SSQ}	DK0	V_{SSQ}	QK0	V_{DDQ}	DQ0	V_{SSQ}	A13
E	V_{SS}	A0	V_{SSQ}	DQ19	V_{DDQ}	QK2#	MF	QK0#	V_{DDQ}	DQ1	V_{SSQ}	CS#	V_{SS}
F	A7	A20	V_{DD}	A2	A1	WE#	ZQ	REF#	A3	A4	V_{DD}	A5	A9
G	V_{SS}	A15	A6	V_{SS}	BA1	V_{SS}	CK#	V_{SS}	BA0	V_{SS}	A8	A18	V_{SS}
H	A19	V_{DD}	A14	A16	V_{DD}	BA3	CK	BA2	V_{DD}	A17	A12	V_{DD}	A10
J	V_{DDQ}	QVLD1	V_{SSQ}	DQ27	V_{DDQ}	QK3#	V_{SS}	QK1#	V_{DDQ}	DQ9	V_{SSQ}	QVLD0	V_{DDQ}
K	DQ29	V_{SSQ}	DQ28	V_{DDQ}	QK3	V_{SSQ}	DK1	V_{SSQ}	QK1	V_{DDQ}	DQ10	V_{SSQ}	DQ11
L	V_{DD}	DQ32	V_{DDQ}	DQ31	V_{SSQ}	DQ30	DK1#	DQ12	V_{SSQ}	DQ13	V_{DDQ}	DQ14	V_{DD}
M	V_{EXT}	V_{SS}	DQ34	V_{SSQ}	DQ33	V_{DDQ}	DM1	V_{DDQ}	DQ15	V_{SSQ}	DQ16	V_{SS}	V_{EXT}
N	V_{SS}	TCK	V_{DD}	TDO	V_{DDQ}	DQ35	V_{REF}	DQ17	V_{DDQ}	TDI	V_{DD}	TMS	V_{SS}

Notes:

1. NF ball for x36 configuration is internally connected and has parasitic characteristics of an address. Ball may be connected to V_{SSQ}.
2. MF is assumed to be tied LOW for this ball assignment.

Ordering Information

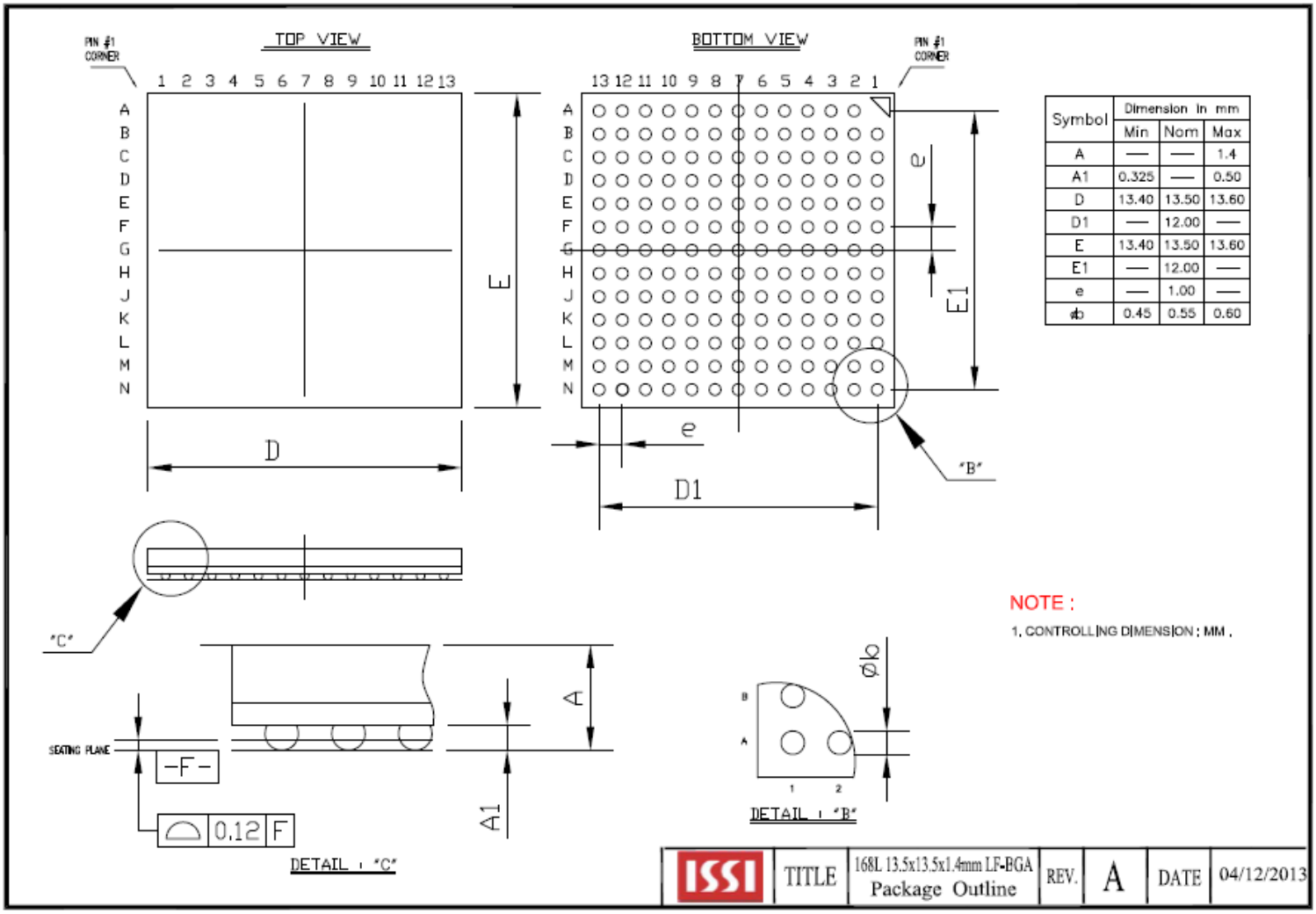
Commercial Range: T_C = 0°C to +95°C

Frequency	Speed (tCK)	tRC(min)	Order Part No.	Organization	Package
933MHz	1.07ns	8.0ns	IS49RL18128-107EBL	128M x 18	168 LFBGA, Lead-free
			IS49RL36640-107EBL	64M x 36	
800MHz	1.25ns	10.0ns	IS49RL18128-125EBL	128M x 18	
			IS49RL36640-125EBL	64M x 36	
		12.0ns	IS49RL18128-125BL	128M x 18	
			IS49RL36640-125BL	64M x 36	

Industrial Range: T_C = -40°°C to +95°C

Frequency	Speed (tCK)	tRC(min)	Order Part No.	Organization	Package
933MHz	1.07ns	8.0ns	IS49RL18128-107EBLI	128M x 18	168 LFBGA, Lead-free
			IS49RL36640-107EBLI	64M x 36	
800MHz	1.25ns	10.0ns	IS49RL18128-125EBLI	128M x 18	
			IS49RL36640-125EBLI	64M x 36	
		12.0ns	IS49RL18128-125BLI	128M x 18	
			IS49RL36640-125BLI	64M x 36	

168-Ball LFBGA Package drawing – 13.5x13.5x1.4mm BGA



Symbol	Dimension in mm		
	Min	Nom	Max
A	—	—	1.4
A1	0.325	—	0.50
D	13.40	13.50	13.60
D1	—	12.00	—
E	13.40	13.50	13.60
E1	—	12.00	—
e	—	1.00	—
øb	0.45	0.55	0.60